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AN ANALYSIS OF
PHASE-LOCKED LOOPS

—————

MARVIN JOSEPH WENIGER

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THESIS

An Analysis of Phase-Locked Loops

by

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Thesis Advisor:

G. J. Thaler

September 1971

Approved for public release; distribution unlimited.

An Analysis of Phase-Locked Loops

by

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Lieutenant, United States Navy
B.S.E.E., University of Idaho, 1963

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ABSTRACT

An investigation was conducted of a third order type two phase-locked loop with a sawtooth phase comparator using both analog and digital simulation techniques and employing an exact system simulation. The results are presented in terms of normalized system parameters and give the system performance as a function of the initial phase between the input and the VCO waveforms, the variation of the input from the VCO frequency, and the system gain and filter characteristics. Some of the data presented includes the time required for the system to meet different types of lock criterion together with the range of frequencies over which the system will lock and the range over which it will lock without cycle skipping.

Investigations were conducted of the system performance for eight different types of phase comparators, of which two of the basic forms had been used previously and the rest were new with this work. It was found that two of the new forms, the R-S nonlinear and the additive with ramp nonlinearity exhibited significantly superior performance in that they possessed increased lock ranges, reduced lock times, and greater values of seize frequency than did the basic systems from which they were derived. It was found that three of the phase comparators yielded an unlimited lock range, even though the lock time became quite long for very large frequency variations.

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I. INTRODUCTION

A. FUNDAMENTAL CONCEPTS OF PHASE-LOCK TECHNIQUES

A phase-locked loop is basically a nonlinear feedback system whose objective is to control the frequency or the phase, the integral of the frequency, of a local oscillator according to a measurement of the error between the phase of the incoming signal and that of the local oscillator.

The basic components of a phase-locked loop are as shown in Figure I-A-1 below. The function of each element is as follows:

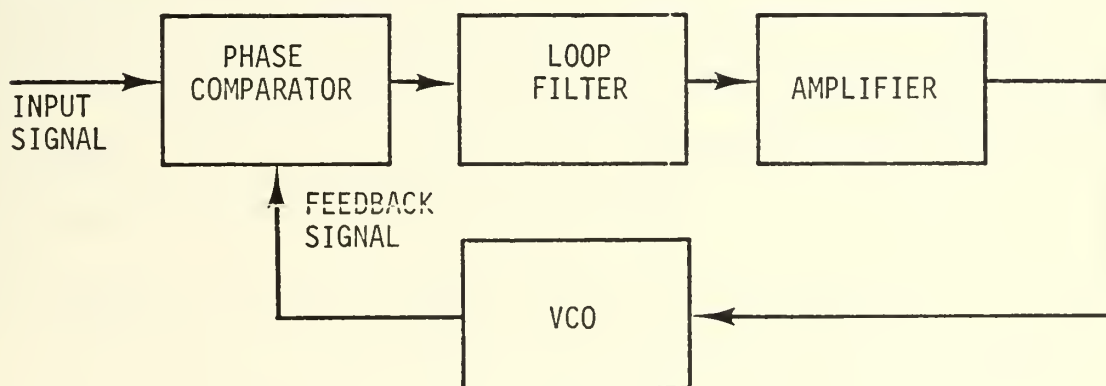


Figure I-A-1. Block Diagram of a Fundamental Phase-Locked Loop.

Phase comparator: This element compares the phase of a periodic input signal with the phase of the voltage-controlled oscillator (VCO) and generates an output which is a measure of the phase difference.

Loop filter: The loop filter filters the output of the phase comparator to get rid of undesired frequency components and develop the desired loop dynamic response characteristics.

Amplifier: The amplifier merely adjusts the system gain to the level required for proper operation.

Voltage-controlled oscillator: The VCO generates a signal whose frequency is dependent upon the input voltage from the filter and amplifier, and is designed such that the voltage input changes the frequency in a direction that reduces the phase difference between the input signal and the oscillator signal.

The phase-locked system shown in Figure I-A-1 is considered locked when the control voltage is such as to maintain the frequency of the VCO equal to the frequency of the incoming signal.

The major difficulties involved in a detailed analysis of the phase-locked system performance are due primarily to the inherent nonlinearity introduced into the system by the phase comparator. It is to better understand the effects of this nonlinearity on the system performance that much of the previous work has been centralized, and it is to this same objective that this report is dedicated.

B. HISTORY OF THE DEVELOPMENT OF THE PHASE-LOCKED LOOP

The techniques of phaselocking have been employed ever since the first two ac generators were synchronized in parallel operation. However, it was not until the early twentieth century that a specific field of study began to develop concerning the concepts and problems of phase-locked systems. As phase-locked devices began to be developed an enormous amount of literature was published concerning the subject, particularly in recent years when the advent of space vehicles equipped with only low power transmitting capability and having a wide range of dopler shifts made the use of fixed tuned receivers impractical.

A complete survey of all the published material covering the theory of phase-locked loops and their wide range of applicability would be

impractical for this thesis. However, a comprehensive list of references has been included to assist those who may desire to delve deeper into some particular aspect. In the remainder of this section an attempt will be made to list only the important milestones, personages, and events which have accompanied the development of the field of phaselock techniques from its beginning to its advanced status at the present time.

The first study of phase-locked loops was accomplished in 1922 by E. V. Appleton [Reference 1] and concerned the use of phase information to lock two oscillators. Then, within ten years, a preview of the more advanced applications was given by H. de Bellescize [Ref. 2] in the first article concerning the use of phaselock in the synchronous reception of radio signals. The communications aspect was again expanded in 1937 when J. R. Woodyard [Ref. 3] investigated the concept of applying what he termed the 'autosynchronized oscillator' to the task of frequency demodulation.

In the 1940's the communications aspect of phase-lock systems took second priority to the then important industrial application of the synchronization of the horizontal and vertical scan in television receivers where phaselocking produced vastly superior performance to the previously used technique of threshold triggering. The primary pieces of literature covering this application were written first by K. R. Wendt and G. L. Fredendall in 1943 [Ref. 4] and soon after by K. Schleslinger [Ref. 5]. However, up to this point in time engineers had been concerned primarily with the applications of phaselocking, and it was not until these applications began to expand to cover phase synchronization in color television that any really significant analytical work was done in the field. Some of the first analytical studies were provided by

T. S. George in 1951 [Ref. 6], W. J. Gruen in 1953 [Ref. 7], and D. Richman in 1954 [Refs. 8 and 9], and all studies pertained to the application of phaselocking to color television.

The greatest obstacle to exact analytical solutions to the problems of phaselocking lie in the inherent nonlinearities of the phase comparator portion of the system. The early method of approach to a solution of the problem involved the use of graphical phase plane methods in an attempt to analyze the operation of the phase-locked loop. This method was characteristic of most of the early work in the field including that of G. W. Preston and J.C. Tellier in 1953 [Ref. 10] and that of W. J. Gruen and D. Richman referred to earlier in Refs. 7-9. More thorough phase plane studies were later pursued by A. J. Viterbi [Ref. 11] and the state of the art in phase plane methods was combined and very completely summarized in a book by A. J. Viterbi [Ref. 12]. However, due to the very nature of phase plane techniques, their particular application to more complex types of problems was limited and other methods of study had to be pursued.

As the applications of phase-locked loops grew it became apparent that an analysis of the system performance by itself was not sufficient and that the effects of noise in the system must also be considered. The first analysis of the performance of the system in the presence of noise appeared in the work of W. J. Gruen [Ref. 7] where a mathematical model of the system in the presence of noise was put forth. This was a linearized model based on the phase relationships, but it provided a new approach which was greatly extended in 1955, two years later, by R. Jaffe and E. Rechtin [Ref. 13]. The work of R. Jaffe and E. Rechtin applied the linear model to show how a phase-locked loop could be used

as a tracking filter for a missile beacon and thereby opened the door leading to some of the more advanced present day applications of phase-locked loops in the field of telemetry. A practical nonlinear model of a phase-locked system in the presence of noise first appeared without proof in a paper by J. A. Develet, Jr. in 1963 [Ref. 14], and this model is still used extensively to the present time, although it has been pointed out recently by C. A. Filippi [Ref. 15] that there are limitations which must be taken into account in its use.

The use of Fokker-Planck techniques to analyze the performance of phase-locked loops in the presence of noise was studied in Russia by V. I. Tikhonov [Refs. 16 and 17] who was able to determine the steady state probability distribution of the first order loop phase error, and he also was able to obtain an approximate expression for the probability distribution when the loop contained a single stage RC filter. A. J. Viterbi [Ref. 18] extended the work of V. I. Tikhonov, and, using Fokker-Planck techniques, he found an exact solution for the first order phase-locked loop system with a sine comparator and was able to obtain the frequency of cycle slipping for the first order loop. Fokker-Planck techniques were then applied to higher order phase-locked loop systems, and W. C. Lindsey [Ref. 19] obtained approximate solutions for the second order system with a sine comparator. However, the probability of obtaining exact solutions for high order systems using this method appears to be poor at present. Nevertheless, the Fokker-Planck method of analysis is still very important, and in 1970 T. L. Steward [Ref. 20] developed a model for a hybrid phase-locked loop using Fokker-Planck techniques. The hybrid loop operated on both the data and the carrier components of the received signal to provide the phase estimate required for coherent detection.

Various other approximation techniques have been applied in an attempt to analyze the complex nonlinearities of the system; the most successful methods are summarized here. In 1957 S. G. Margolis [Ref. 21] analyzed the nonlinear operation in the presence of noise by perturbation methods, obtaining a series solution for the loop differential equation, and, using only the first few terms of the series, he determined the approximate moments of the phase error. Several years later R. D. Barnard [Ref. 22] studied the capture in phase controlled oscillators through the application of variational techniques. Methods similar in concept to those used by S. G. Margolis were applied by H. L. Van Trees [Ref. 23] when he obtained a Volterra Series representation of the closed-loop response by a perturbation method, but with the advantage of his simplified model he was able to obtain more extensive results. About this same time C. R. Cahn [Ref. 24] performed a piecewise linear analysis to determine the behavior of phase-locked loops employing square wave rather than sinusoidal signals, resulting in triangular rather than sinusoidal nonlinearities. The results were qualitatively and quantitatively similar to those found previously for sinusoidal loops.

So far almost all of the research discussed has been concerned with low order systems employing a sinusoidal phase comparator, and the literature on the topic has been limited to articles on specific aspects scattered throughout the various technical journals. At last in 1966 three publications were provided which served to compile the results of much of the previous work on phase-locked loops using sinusoidal phase comparators into a convenient and quite comprehensive body of reference material. Two of these publications were books, one by F. M. Gardner [Ref. 25] and the other by A. J. Viterbi [Ref. 12], which provided

comprehensive summaries of the theory and communication oriented applications of the principles of phase-locked loops. The third publication was provided by R. C. Tausworthe [Ref. 26], and this provided a handbook method of approach to the design and testing of sinusoidal phase-lock receiver systems.

The study of phase-locked loops has not been restricted to the use of a sinusoidal phase comparator, and as the application of phase locked loops began to extend to the utilization of pulse and digital waveforms, interest in other forms of phase comparators grew. A. J. Goldstein [Ref. 27] and C. J. Byrne [Ref. 28] have investigated the sawtooth phase comparator and have produced an extensive amount of theoretical and experimental information pertinent to this comparator. The sawtooth phase comparator was investigated because of the advantage it had in a linear output over a wider range of phase error. Just recently E. N. Protonotarios [Ref. 29] presented an exact graphical method for the evaluation of the number of slipped cycles and the pull in time for a phase-locked loop using a sawtooth comparator. Also in 1962 L. M. Robinson [Ref. 30] developed the Tanlock phase comparator, which was another approach to the problem of linearizing the operations of the sinusoidal comparator. Improvements were made to the Tanlock system and the technique was extended to the N^{th} order in 1966 by J.C. Lindenlaub and J. J. Uhman [Ref. 31]. Results of further work by these same two engineers in studying the lock range of the modified N^{th} order Tanlock phase comparator in the presence of noise was presented in Ref. 32. In the same basic category as the above, research was done by B. J. Leon and L. L. Cleland [Ref. 33] who studied the effects of modifying the phase comparator by the proper insertion of additional controlled nonlinearities in an attempt to improve the operational characteristics.

Since the very beginning work with phase-locked loops, one of the primary goals has been to obtain as wide a frequency range as possible over which the system will lock. Modifications to the filter and phase comparator have been tried in an effort to accomplish this result. Another approach consisted of sweeping the local oscillator over a specified range of frequencies until a lock resulted. Analysis of work done using this technique was provided by R. A. Dye in Ref. 34. Other techniques include the use of phase subtraction to extend the range of the phase-locked demodulator as studied by A. Acampora and A. Newton [Ref. 35], and the use of a dual mode of control by C. F. Suter, Jr. [Ref. 36], where synchronization was obtained over a broad range in two steps. In the dual mode system frequency differences were first used to obtain corrections for wide frequency range differences, and phase characteristics were used to obtain final synchronization. The most recent and perhaps most radical techniques for improving the lock-on range of a phase-locked loop was put forth by G. L. Baldwin and W. G. Howard in 1969 [Ref. 37] where the approach used was to eliminate the loop filter and use harmonic cancellation in its place. Further work will be required to serve judgement on the practicality of this technique.

Some aspects of phase-locked loops have always been of interest, such as the phenomenon of cycle slipping which has been studied from the start and which is still being pursued as evidenced by the recent works of J. J. Uhlan, Jr. [Ref. 38] and R. C. Tausworthe [Ref. 39]. Another topic which is both old and new is the concept of preceeding the phase-locked loop by bandpass limiters. This concept was first referred to in 1955 by R. Jaffe and E. Rechtin in Ref. 13 and again in 1958 by W. C. Lindsey [Ref. 40].

One concept which had not been pursued thoroughly in the past, due to the complexity associated with it, was that of increasing the order of the loop transfer function. One good analysis that has recently been published is that by R. S. Hebbert and D. J. Burton [Ref. 41] where the authors found that the third order system would acquire a sine wave automatically in approximately the same time required for a frequency swept second order system of the same noise bandwidth. This implies that increasing the order of the system might be very beneficial under certain conditions.

While analog phase-locked loops are already widely used in communications systems, the increasing importance of digital signals in communications, control, and computer applications together with the advent and larger utilization of integrated digital circuitry and of the digital computer itself, has led to a growing need for a digitized version of the phase-locked loop. Some researchers into this subject, such as E. M. Drogen [Ref. 42] and W. E. Larimore [Ref. 43], have simply replaced the continuous filter with a digital filter, and W. E. Larimore commented on the advantages that are provided in that the digital filter can be made adaptive to enable more efficient and more flexible operation in the presence of interference or jamming. Other approaches have been to use both a digital filter and a digital VCO as was done first by P. R. Westlake [Ref. 44], who produced the first real study of the application of digital techniques to phase-locked loops, and later by F. D. Natali [Ref. 45]. Natali's model indicated improved performance under low frequency operation such as when applied in digital bit synchronization, and he capitalized on one of the advantages of a digital VCO which is improved stability. L.F. Judd [Ref. 46] applied Z-transform analysis of a partially digital loop with a sawtooth comparator, using a digital counter to reduce the

feedback frequency of the VCO to within one cycle of the reference frequency so that the final signals applied to the phase comparators were a train of pulses of almost equal frequency. The problem, however, as demonstrated by S.C. Gupta [Ref. 47], was more complicated than simply substituting digital blocks for analog blocks in the phase-locked loop. Gupta showed that if the analog filter were replaced by a digital filter, the order of the optimum filter was one degree higher than the order of the optimum filter in the analog case; thus pointing out clearly that if the technique were simply to discretize the analog filter, the result cannot be optimum. The most comprehensive and recent work on digital phase-locked loops was performed by G. Pasternack and R.L. Whalin [Ref. 48]. In their phase-lock loop system no low pass filter or VCO is required. The basic component of the loop is an exclusive-or comparator which develops an output gating function which is dependent upon the phase relationships of its inputs. This system gives assured high stability and makes the system ideal for microminiaturization. Of course miniaturization is not limited to the digital aspect of phase-locked loops, and integrated circuit phaselock packages which will perform a wide variety of tracking and demodulation tasks are becoming commercially available to the designer.

The material discussed so far has concerned changes within the loop itself which were designed to give better performance. However, the changes need not be restricted to the system's internal components, and both J.J. Stiffler [Ref. 49] and J.W. Tayland [Ref. 50] have studied the problem of selecting the input and VCO signals so as to minimize the tracking errors due to additive noise.

While a complete historical coverage of all the work accomplished in the field of phase-lock techniques would not be feasible here, the above

summary should serve to highlight the principle accomplishments in the various regions of endeavor and provide a starting point for further research into any particular aspect of interest to the reader.

C. APPLICATIONS OF PHASE-LOCKED LOOPS

Phase-locked loops play an important role in modern day electronics. Some of the uses of the phase-lock technique have been mentioned briefly in the earlier portions of this treatise, and an overview of all the major applications will be given here.

1. Television

By far the most commonplace utilization of a phase-locked loop is in the standard home television set where phase locking is used in the synchronization of the horizontal and vertical scans and has proven much more satisfactory than the earlier technique of using threshold triggering to synchronize a local oscillator with the incoming signal. Later, color was added to a monochrome picture by means of a narrow band signal which carried the hue of the color in its phase and the color saturation in its amplitude. In order to provide a phase reference, a short burst of oscillations at the color subcarrier frequency was provided during the retrace interval, and this burst was used to phaselock the receiver to the transmitted signal.

2. Communications

The advent of space satellites placed an added emphasis on an old communications problem, that of detecting a weak signal in the presence of strong noise. However, due to the low power capability of space vehicles, the problem was now of such magnitude that the conventional wideband receiver was incapable of solving it, and phase-locked receivers appeared to be the only answer available. The phase-locked loop has served many functions in the development of the communications receiver,

the first of which was simply as a tracking filter added to the output of a receiver. In this receiver a local oscillator was mixed with the incoming signal to produce a beat frequency which was strongly imbedded in noise. A phase-locked loop was then used at the output of the receiver to track the beat frequency. The disadvantage of this system lies in the fact that the receiver bandwidth must be made wide enough to cover the entire range of dopler frequency shift plus frequency changes due to transmitter instabilities, thus giving a very wide noise bandwidth. Contrasted to the above situation, where most of the receiver was outside the phase-locked loop, is the more recent development where the entire receiver is within the phase-locked loop and the local oscillator is varied to maintain a constant frequency into the IF amplifier. This results in a truly narrow-band system throughout the IF amplifiers and bandpass filters, and as a result the noise bandwidth is reduced significantly. The control voltage applied to the VCO can be used to measure the amount of dopler shift and determine the relative velocity changes in the transport media.

A phase-locked loop may also be used in receiver automatic gain control circuits by passing the receiver output through a phase-locked loop to obtain a coherent reference, and then using this reference together with the receiver output in a synchronous amplitude detector followed by a very narrow-band filter to obtain the feedback voltage. The output of the filter may be used to control the receiver gain very effectively since it is due chiefly to the presence of the signal and is very insensitive to noise. This is in contrast to the more common AGC circuit which is equally sensitive to signal or noise.

In pulse code modulated communications systems the phase-locked loop has been found to be very effective both as a bit synchronization

device to make the clock of the data processing mechanism coherent with the bit rate, and as a means of smoothing out the random jitter which may occur in the digital signal.

Another common application of the phase-locked loop in communications systems is in the area of signal demodulation, where its use was originally limited to frequency demodulation, but has since been extended to all forms including AM demodulation. When a phase-locked loop is locked on to an incoming FM signal, the VCO of the loop varies in frequency so that it tracks the incoming frequency. Under these conditions the filtered error voltage which forces the VCO to maintain lock corresponds to the FM signal and represents the desired demodulated output. The linearity of the demodulator depends upon the linearity of the VCO voltage-to-frequency conversion characteristics, and can be made quite good over the desired range, thus giving a higher degree of detection linearity than other methods available. Changes in the phase of the transmitted signal may also be detected by similar methods. Data transmission is sometimes accomplished using frequency-shift keying where the transmitted signal is shifted between two distinct frequencies. Here the voltage to the VCO shifts between discrete voltage steps which correspond to the demodulated binary information. In many FM receivers the functions of frequency tracking and frequency demodulation are combined and accomplished within a single phase-locked loop which makes up the complete receiver system.

The phase-locked loop can also be used as a coherent detector for demodulating AM signals. The operation is similar to that of the AGC system described earlier and uses the phase-locked loop to obtain a signal of the same frequency as the AM carrier but containing no amplitude modulation. The output of the VCO is then multiplied with the incoming

signal and passed through a low-pass filter to obtain the demodulated output. The phase-locked loop AM detection system exhibits a high degree of selectivity, and, due to its coherent nature, it offers a higher degree of noise immunity than conventional peak detection AM demodulators.

3. Frequency Generation

It is often not possible to get the desired frequency stability at the required power level, as in crystal oscillators where the best long-term frequency stability occurs when operated at low RF power levels, and the best short-term phase stability occurs when operated at medium power levels. However, a satisfactory system can be obtained by locking a very low-level and a medium-level crystal oscillator together using a phase-locked loop. In the microwave region there are several oscillators which are capable of providing moderate levels of power output, including klystrons, voltage-tuned magnetrons, backward-wave oscillators, and even triodes. These devices all have the common drawback of poor frequency and phase stability, but they have the advantage that it is relatively easy to adjust their output frequency. Thus these microwave oscillators can be stabilized by locking them to a harmonic of a low-frequency stable oscillator using a phase-locked loop and thereby obtaining the required frequency and phase stability. In this way also a noisy oscillator may be cleaned up by using a phase-locked loop with a wide bandwidth, and a large reduction in the phase jitter of the system is obtained.

Frequency multiplication and division may be used with phase-locked loops to generate output signals which are multiples of the input frequency. This can be accomplished by locking the VCO to the n^{th} harmonic of the input to give frequency multiplication or by locking the

m^{th} harmonic of the VCO to the input to give frequency division. Frequency division or countdown circuits may also be placed in the system to give similar effects without the use of harmonics.

Frequency translation is readily accomplished using a phase-locked loop to translate the frequency of a stable fixed-frequency oscillator by a small amount. The fixed oscillator is mixed with the VCO to yield a beat frequency which is put into a phase comparator together with another oscillator whose frequency is set to the value of the desired offset. The phase-locked loop is then closed back to the VCO whose frequency is automatically varied until the beat frequency equals the required offset. Thus the output of the VCO is a stable signal whose frequency is the sum of the stable oscillator plus the frequency of the offset oscillator. This method of frequency translation avoids the critical circuit and filter adjustments which would have been required if the translation had been accomplished using conventional sideband techniques.

The principles of frequency multiplication, division, and translation discussed above can be combined to form a completely coherent frequency synthesizer based on a single extremely stable fixed frequency oscillator and the use of phase-locked loops.

4. Digital Data

When transferring digital data, either between remote installations or between units within the same facility, it is mandatory that exact synchronism be maintained within the sending and receiving units. The phase-locked loop is frequently used with digital systems to obtain bit synchronization and to synchronize the clocks of two interacting systems. Phase-locked loops are also used to synchronize disc and tape drive mechanisms for the transfer and storage of data in digital

systems, and a phase-locked loop with a wide bandwidth filter can be used to eliminate phase jitter in a digital pulse train.

5. Phased Arrays

Normally, a very high antenna gain requires a large aperture antenna which in turn requires extremely close tolerances in physical construction to avoid unwanted phase shifts. The close tolerances required serve to greatly increase the cost of the antenna. However, if phase-lock techniques are applied to the output of several smaller antennas, it is possible to compensate for the effects of unwanted phase shifts and as a result a very large effective aperture may be attained without the close tolerances normally required. Phase-locked loops may also be used to obtain automatic steering of antenna arrays and to obtain adaptive control of antenna arrays. Phase-lock control of phased array antennas has been successfully used aboard a space vehicle to automatically track a ground station. Since the concepts of phased arrays apply to underwater sound reception as well as to electromagnetic reception, similar phase-lock techniques might be applied to the reception and tracking of underwater sound signals.

6. Miscellaneous Applications

Phase locking has been used successfully to synchronize the oscillation of two lasers and also to synchronize a laser to a harmonic of an RF oscillator. Since the major advantage of a laser is the coherence of its emitted signal, it is necessary to employ a coherent receiver rather than a simple power detection receiver if full advantage is to be made of the coherent source. Research is presently being conducted on the concept of coherent laser communication systems with the possible results of a completely new concept of communications for the future.

Long-range radio navigation systems employing low frequencies and phase-lock techniques to detect slight phase differences in received signals are currently being investigated. The phase-locked loop is well suited to this purpose since it is capable of operation at very low frequencies. Other navigation applications include the use of phase-locked loops for determining the radial velocity of a moving vehicle by measuring its dopler shift, with this measurement frequently requiring the use of a coherent transponder on one of the vehicles, particularly if the vehicle whose speed is to be measured is a space vehicle. The coherent transponder receives the transmitted signal and transmits a reply at a rational multiple of the received signal while maintaining coherency throughout the process so that the phase of the returned signal may be compared with the phase of the transmitted signal to determine the dopler shift.

Since the applications of phase-locked loops are numerous, it has only been possible here to discuss some of the more common areas in which they are utilized, and thus to provide an overview to their status in modern technology. As research provides additional information concerning the basic operation and locking characteristics of the loops under various operating conditions, and as the performance of the phase-locked loop is improved, it is certain that additional and more advanced applications will be discovered.

II. SYNOPSIS OF SIGNIFICANT ANALYTICAL TECHNIQUES AND RESULTS

Within the past twenty years there has been a huge volume of material published on the concepts of phase-lock techniques. Much of the material has been referred to earlier when discussing the history and growth of this new field, and no further effort will be made here to follow the historical progress of the various methods of approach. Instead, an attempt will be made to provide a synopsis of the analytical techniques and results which have proven most useful to an understanding of the operation of phase-locked loops and for system design using phase locking. When several techniques have been proposed for the same problem, the selection of methods for presentation here was based not only on the most recent accomplishments, but also on the exactness and range of applicability of the techniques. When an alternative exists, a single generalized form of the results will be given rather than providing several specific formulations. Due to the nature of the nonlinearities involved, there are very few purely analytical results available for higher order systems. However, there has been a significant amount of simulation work done in this area which has helped researchers obtain a feel for the system's operation, and while no formulas can be presented for this type of work, an effort will be made to discuss some of the important results. No actual derivations will be given here since their inclusion would require an exorbitant amount of space, and since this information can readily be obtained from the reference literature. What will be provided in each case is a brief discussion of the aspects of the particular problem, the solution, and a discussion of the applicability of the results.

A. SOLUTIONS BASED ON LINEAR APPROXIMATIONS

A generalized block diagram for a phase-locked loop is shown in Figure II-A-1.

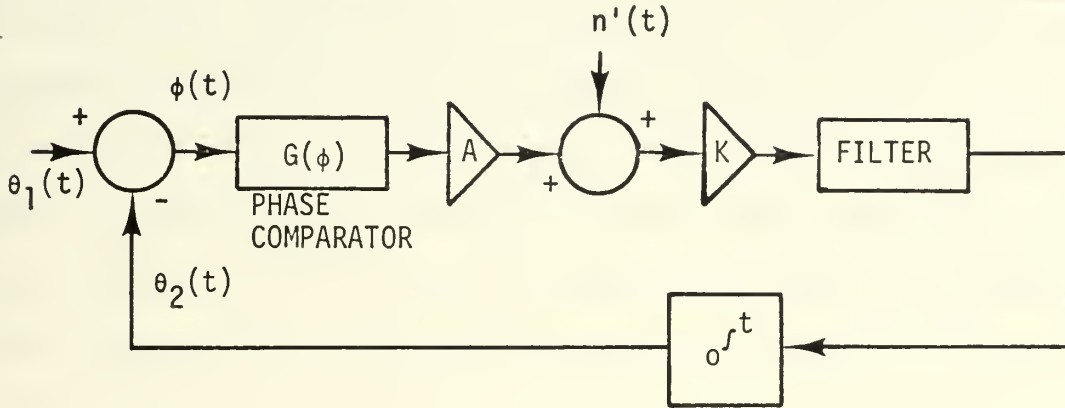


Figure II-A-1. Model of a Phase-Locked Loop

This figure allows for the use of any type of phase comparator and for either a linear or nonlinear filter. If the input signal to the actual system is any periodic function of $(\omega_0 t + \theta_1(t))$ and the signal from the VCO is also a periodic function of $(\omega_0 t + \theta_2(t))$, then the operation of the system may be expressed in terms of the input and output phases $\theta_1(t)$ and $\theta_2(t)$ as shown in Figure II-A-1. For the most common applications where sinusoidal input and VCO signals are used together with a sine phase comparator, and if the input is corrupted by narrowband Gaussian noise $n(t)$ with zero mean and one sided spectral density of N_0 watts per hertz where:

$$n(t) = \sqrt{2} [n_1(t) \sin \omega_0 t + n_2(t) \cos \omega_0 t] \quad (\text{II-a-1})$$

then after the phase comparator this noise will have the form

$$n'(t) = -n_1(t) \sin \theta_2(t) + n_2(t) \cos \theta_2(t) \quad (\text{II-a-2})$$

and therefore may be added into the block diagram as shown in Figure II-A-1.

The usual forms of the phase comparator such as the sine, sawtooth, and tanlock all have a region of operation for small phase errors over which the action of the phase comparator is essentially linear. Similarly, the loop filter is almost always a linear filter, and if the additional constraint is added to require the system to operate in a noise free environment so that $n'(t)$ is zero, then the complete loop may be approximated as a linear system. This approximation greatly simplifies the system analysis since it allows the phase-locked loop to be treated as a normal feedback system using Laplace transform techniques yielding a closed-loop transfer function of

$$H(s) = \frac{\theta_2(s)}{\theta_1(s)} = \frac{AK F(s)}{s + AK F(s)} \quad (\text{II-a-3})$$

and a phase error of

$$\phi(s) = [1 - H(s)] \theta_1(s) \quad (\text{II-a-4})$$

The steady state phase error for the linearized model of the phase-locked loop for various loop filters with both a constant input frequency and an input frequency which is changing at a constant rate is shown in Table II-A-I. The type 0 system is not included in Table II-A-I because it is difficult to obtain due to the integration in the VCO, and because even if a filter were provided which would force the system to type 0 it would result in an infinite error to all inputs. From the table it can be observed that a first order loop is limited to applications where the input frequency is constant, while the third order type three system gives zero steady state error for all inputs listed and obtains often needed versatility at the expense of system complexity. As will be seen later, exact solutions for the third order loop are very difficult to obtain. It must be remembered that all computations discussed above are limited to small deviations of the phase error.

Order of Loop	Type Number of Loop	Filter Transfer Function	Closed Loop Transfer Function	Steady State Phase Error For a Constant Frequency Input Given by $\theta_1(t) = (\omega - \omega_0)t + \theta_0$	Steady State Phase Error When the Input Frequency is Changing at a Rate \bar{R} radians/sec ² $\theta_1(t) = \frac{1}{2} \bar{R} t^2 + (\omega - \omega_0)t + \theta_0$
1st	1	1	$\frac{AK}{S + AK}$	$\frac{\omega - \omega_0}{AK}$	∞
2nd	1	$\frac{s+a}{s+b}$	$\frac{AK(s+a)}{s^2 + (AK+b)s + AKa}$	$\frac{b(\omega - \omega_0)}{aAK}$	∞
	2	$1 + \frac{a}{s}$	$\frac{AK(s+a)}{s^2 + AKs + AKa}$	0	$\frac{R}{AKa}$
3rd	1	$\frac{(s+a)(s+b)}{(s+c)(s+d)}$	$\frac{AK(s+a)(s+b)}{s^3 + (c+d+AK)s^2 + (cd+aAK+bAK)s + AKab}$	$\frac{(\omega - \omega_0)cd}{AKab}$	∞
	2	$\frac{(s+a)(s+b)}{s(s+c)}$	$\frac{AK(s+a)(s+b)}{s^3 + (c+AK)s^2 + (a+b)AKs + AKab}$	0	$\frac{Rc}{AKab}$
	3	$1 + \frac{a}{s} + \frac{b}{s^2}$	$\frac{(s^2 + as + b)AK}{s^3 + AKs^2 + AKas + AKb}$	0	0

Table II-A-I. Steady State Phase Error for a Linearized Phase-Locked Loop as a Function of Loop Order, Type Number, and Filter Transfer Function.

B. SINE COMPARATOR SYSTEMS IN THE ABSENCE OF NOISE

For the sine phase comparator, which is most frequently used with sinusoidal input and VCO signals, the phase comparator function $G(\phi)$ of Figure II-A-1 is given by

$$G(\phi) = \sin \phi(t) \quad . \quad (\text{II-b-1})$$

Under these conditions it is possible to write the exact time domain equation for the phase locked loop as

$$\frac{d \phi(t)}{dt} = \frac{d \theta_1(t)}{dt} - AK \int_0^t f(t-u) \sin \phi(u) du \quad (\text{II-b-2})$$

where $f(t)$ is the impulse response of the loop filter.

Since the second-order loop is used most frequently, an analysis will be made for a second order type two system using a filter

$$F(s) = 1 + \frac{a}{s} \quad (\text{II-b-3})$$

and a constant frequency input with

$$\theta_1(t) = (\omega - \omega_0)t + \theta_0 \quad . \quad (\text{II-b-4})$$

Under these conditions Equation II-b-2 becomes

$$\frac{d^2 \phi}{dt^2} + AK \cos \phi \frac{d\phi}{dt} + a AK \sin \phi = 0 \quad (\text{II-b-5})$$

which can be further reduced to

$$\frac{d\dot{\phi}}{d\phi} = -\cos \phi - a' \frac{\sin \phi}{\dot{\phi}} \quad (\text{II-b-6})$$

by letting $\tau = tAK$ and $a' = a/AK$. Equation II-b-6 is a phase-plane equation and represents the system exactly. Viterbi [Ref. 12] provides a comprehensive summary of graphical analysis using the phase-plane approach.

If both sides of Equation II-b-6 are multiplied by $\dot{\phi}$ and integrated between the limits $-\pi$ to $+\pi$, then substitution for $d\dot{\phi}$ will result in

$$\frac{1}{2} [\dot{\phi}^2(\pi) - \dot{\phi}^2(-\pi)] = -\frac{a'}{2} \int_{-\pi}^{\pi} \frac{1 - \cos 2\phi}{\dot{\phi}} d\phi . \quad (\text{II-b-7})$$

This result is important because it demonstrates that for each cycle of width 2π the value of $|\dot{\phi}|$ must decrease, and this implies that the pull-in range for a perfect second order type two loop in the absence of noise is infinite.

For the same conditions as above it is possible to obtain the approximate pull-in time, or time to lock, subject to the assumptions that the initial frequency error is large ($\dot{\phi}(0) \gg 1$) and that the change in frequency per cycle is small. The pull-in time is denoted by t_p where

$$t_p \approx \frac{1}{a} \left[\left(\frac{\omega - \omega_0}{AK} \right) - \sin \theta_0 \right]^2 . \quad (\text{II-b-8})$$

Therefore, even though the pull-in range may be infinite, the time required to achieve frequency lock may be prohibitively large if the initial frequency is large compared with the loop gain.

Now consider a second-order loop with an imperfect integrator where the filter transfer function is given by

$$F(s) = \frac{s + a}{s + \epsilon} . \quad (\text{II-b-9})$$

Here the system is of type one and no longer can pull-in be guaranteed for all frequencies. In fact it has been shown in Ref. 12 that if

$$\omega - \omega_0 > \frac{aAK}{\epsilon} \quad (\text{II-b-10})$$

pull-in can never occur; even for values of $\omega - \omega_0$ less than the maximum, pull-in is not always certain. An approximate analytical solution based on the assumption that $\dot{\phi}(0)$ is large shows that pull-in will always occur when

$$\omega - \omega_0 < 2AK \left[\frac{a}{AK} \left(1 - \frac{AK}{2\epsilon} \right) \right]^{\frac{1}{2}} \quad (\text{II-b-11})$$

so that now an upper and a lower bound has been provided.

If the input frequency were changing at a constant rate it was seen from Table II-A-I that the only second order loop which could track the input signal would be a type two system, and even this would always have a finite phase error. Furthermore, it has been found that the system would never attain lock, or if in lock it would immediately fall out of lock if

$$R > aAK \quad (II-b-12)$$

where R is the rate of frequency change in radians per second squared. This also places an upper bound on the sweep rate for a system where the VCO is swept through a band of frequencies to aid in obtaining lock. In fact, experimental data has shown that acquisition is certain only at sweep rates of less than one half of the maximum.

Exact solutions do not exist for third order systems; however, Viterbi [Ref. 12] has shown that for a loop filter of

$$F(s) = 1 + \frac{a}{s} + \frac{b}{s^2} \quad (II-b-13)$$

which yields a third order type three system, the loop is always unstable for

$$\frac{b}{AK^2} \geq \frac{1}{2} \quad (II-b-14)$$

Furthermore, for a linear frequency variation there is a region

$$\frac{R}{aAK} < 1 \quad (II-b-15)$$

where the tracking behavior of the third order loop does not vary much from that of the second order loop; but for

$$\frac{R}{aAK} \geq 1 \quad (II-b-16)$$

which is the region where the second order type two loop cannot lock on, there exists a limited range where a proper choice of the parameter b enables the third order system to lock satisfactorily.

Other research conducted on the third order system [Ref. 41] has used the approximation that for large frequency differences and for long periods of time the highest order integral is the dominant term in the output of the loop filter with a dc input. Using this approximation it has been shown that for the third order system the time to lock was approximately a function of the frequency difference, while for a second order system the time to lock was a function of the frequency difference squared. Thus for a large frequency difference the time to lock for a third order system is significantly less than that of a second order system. Using the same approximation as above but utilizing a triangular phase comparator instead of the sine comparator, it was found that the time to lock for a third order system could be further reduced by a factor of 0.78. This information tended to support the concept that there were specific advantages to a third order phase-locked loop for certain applications.

A relation for the pull-in range of a phase-locked loop which is not limited by the order of the loop was derived by J.R. Woodbury in Ref. 51. The approach used was to first assume that the loop input frequency is outside the pull-in range and then determine the smallest value of the input error frequency for which a steady asynchronous state exists. Another powerful aid used in the derivation was the assumption that, when outside of the pull-in range, the phase error voltage could be considered as a periodic function whose frequency was the difference between the input signal and the average frequency of the VCO. Once this assumption is made, it is possible to represent the phase comparator output voltage by a Fourier series, and truncating the series by assuming that only the fundamental and second harmonic terms of the series need be considered due to the action of the low-pass filter, a combination can then be made

of the Fourier series expansion with the system equations to determine an expression for the periodic frequency ω_d from the phase comparator. Using this expression it is possible to determine the relationships for which no real solution for ω_d exists, which is the criterion from which an equation for the pull in frequency ω_p may be expressed as

$$\omega_p^2 = 2 \omega_m^2 (1 - \Delta_0) \operatorname{Re} \left[H \left(\frac{j\omega_p}{2} \right) \right] \quad (\text{II-b-17})$$

where ω_m is the peak frequency excursion of the VCO from ω_0 and Δ_0 is an elaborate expression consisting of the filter characteristics, ω_m , and ω_d . For any order phase-locked loop using a sine comparator, Equation II-b-17 can be solved for ω_p by straight forward solution techniques. The important thing is that in this solution the only assumptions and approximations made are in the Fourier series approximation of the phase comparator output, and the order of the system has not been limited in any way. Unfortunately, no information regarding pull-in time is available by this method.

C. SINE COMPARATOR SYSTEMS CORRUPTED BY NOISE

In actual physical systems there is no such thing as a noise-free signal. All signals contain a certain amount of noise, and although it is possible that under some conditions the noise will be so small in comparison to the signals that it may truly be disregarded in the system analysis, it is certain that in many systems the noise will significantly effect the operation. An exact analysis of the phase-locked loop in the presence of noise was not available until some time after the systems attained wide commercial use, and even now exact analytical solutions exist only for the most elementary systems and for limited aspects of more complicated systems. A wide variety of analysis techniques will be presented, some of which are relatively old but which are still considered

important, not because of their historical value but because their special methods and models still provide valid solutions for particular types of phase-locked loop applications.

When using completely linearized models an indication of the system performance in a noisy environment may be obtained by considering the loop-noise bandwidth which is defined by

$$B_L = \frac{1}{2\pi} \int_0^\infty |H(j\omega)|^2 d\omega \quad (\text{II-c-1})$$

where the notation of Figure II-A-1 is used. The loop-noise bandwidth can then be applied to the calculation of the variance of the phase error by

$$\sigma_\phi^2 = \frac{N_o B_L}{A^2} \quad (\text{II-c-2})$$

and from this it is seen that increased loop-noise bandwidths yield a greater variance in the system output.

An early model of a phase-locked loop in the presence of noise was provided by H.L. Van Trees [Ref.52]. The system and his particular model are shown in Figure II-C-1 Part (a) and Figure II-C-1 Part (b) respectively. Using this model the effect of noise on the mean and the variance of the phase error was studied and upper bounds on the stability limits were obtained. By employing a linearized model where $\sin \phi \approx \phi$, it was found that for a first order loop the mean of ϕ became unbounded for large time when

$$N_o > \frac{2}{K} \quad (\text{II-c-3})$$

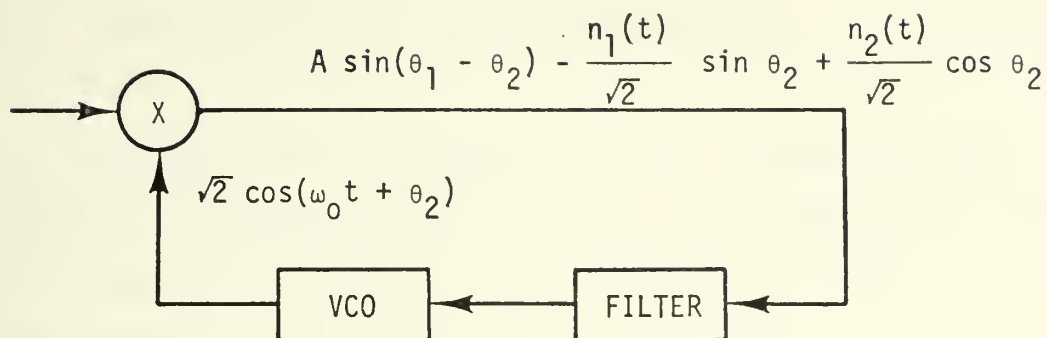
and the variance became unbounded for large time when

$$N_o > \frac{1}{K} \quad (\text{II-c-4})$$

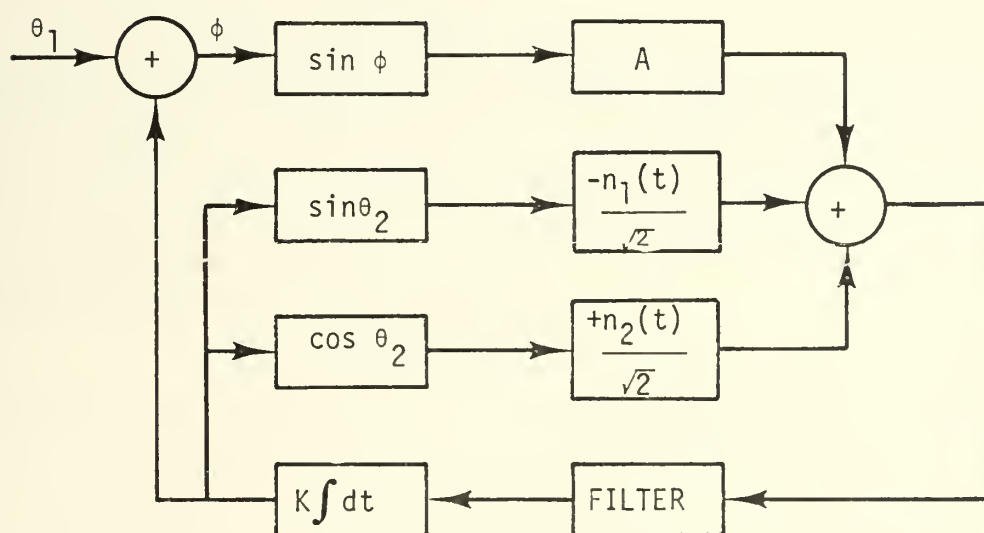
where K is the gain of the VCO. It should be noted that these are only upper bounds.

For a second order system Van Trees developed results which were accurate only for moderate values of KN_o . Under these operating

$$\sqrt{2} A \sin (\omega_0 t + \theta_1) + n_1(t) \sin \omega_0 t + n_2(t) \cos \omega_0 t$$



(a) Block Diagram of a Phase-Locked Loop with Narrowband Additive Noise at the Input.



(b) Model of the System Shown in Part (a)

Figure II-C-1. Block Diagram and Corresponding Model of a Phase-Locked Loop with Narrowband Additive Noise at the Input

conditions and using the linear approximation of the phase comparator, it was found that the upper bound for stability to exist required that

$$N_0 < \frac{1}{K} \quad (II-c-5)$$

J.A. Develet [Ref. 14] developed a simple approximate theory for the threshold of a phase-locked loop using the quasi-linearization techniques of R.C. Booton, Jr. [Ref. 53]. The approach was to replace the nonlinear element by an equivalent gain K_A which was the average gain of the nonlinear device under the expected operating conditions. For the sinusoidal comparator K_A may be determined by

$$K_A = \int_{-\infty}^{\infty} g'(x) p_1(x) dx \quad (II-c-6)$$

where $g'(x)$ is the derivative of the phase comparator function, and $p_1(x)$ is the probability of the phase error $\phi(t)$ which must be Gaussian to conform to Booton's criterion. The equivalent gain can also be expressed in terms of the phase error variance by

$$K_A = E \exp [-\sigma^2/2] \quad (II-c-7)$$

where E is the gain of the sinusoidal phase comparator. The variance can be expressed as a function of modulation error and noise error, and then solved for the received power as a function of the loop transfer function $\theta_2(\omega)/\theta_1(\omega)$. The system can be optimized for maximum receiver output and if the transfer function is expressed as

$$\frac{\theta_2(\omega)}{\theta_1(\omega)} = A(\omega) \exp [j \theta(\omega)] \quad (II-c-8)$$

then the maximum receiver sensitivity occurs for

$$A(\omega) \Big|_{OPT} = \frac{\phi_m(\omega)}{\phi_m(\omega) + \frac{\phi_n(\omega) \exp[\sigma^2]}{2 S_{if \min}}} \quad (II-c-9)$$

where ϕ_m and ϕ_n represent the one sided power spectral density of the signal and noise respectively. The same result can be obtained by minimizing either the received signal power or the phase error variance.

In order to test the performance of the quasi-linear receiver model in the presence of white Gaussian noise it is just necessary to replace ϕ_m by $\phi_{if} \exp[\sigma^2/S_{if}]$ where ϕ_{if} is the receiver noise density, and obtain the fundamental relationship

$$\sigma^2 = \frac{\phi_{if} \exp[\sigma^2]}{S_{if}} \int_0^\infty \log_e \left(1 + \frac{S_{if} \phi_m(\omega)}{\phi_{if} \exp[\sigma^2]} \right) d\omega . \quad (\text{II-c-10})$$

This important result indicates that if given a receiver output quality constraint and a receiver noise density, there would not be a bounded solution for the variance if the received power S_{if} were too small. The limiting value of S_{if} is the threshold for this quasi-linear model. These formulas were then applied to a bandlimited phase-encoded white Gaussian signal using an optimum receiver, and also to a second-order loop receiver. The results were shown graphically in Ref. 14. However, the limitations of this technique must be considered, in that the results are only applicable for large values of signal to noise at the system input.

The Volterra functional expansion technique is a generalization of the convolution integral and was applied to the analysis of the non-linear phase-locked loop in the presence of noise by H.L. Van Trees [Ref. 54]. The nonlinear function was represented as a sequence connected in parallel where the impulse response of each path is called a kernel. The kernel has special properties which enable it to be easily calculated, and once it is obtained for a system it remains constant regardless of the system's input signal.

By applying this technique to a first order loop with a constant frequency input and approximating the system by using only the first five kernels, the phase error variance was found to be

$$\langle \phi_{(5)}^2(t) \rangle \approx Z + \frac{1}{2} Z^2 + \frac{13}{24} Z^3, \quad (\text{II-c-11})$$

where

$$Z = \frac{KN_0}{4A^2} \quad (\text{II-c-12})$$

and A is the rms value of the input signal. This Z has been called the coherent loop noise-to-signal ratio. The results obtained by using Equation II-c-11 agree closely with the exact solution for the first order loop obtained by V. I. Tikhonov in Ref. 16.

For a second order loop with no modulation, an approximation using only the first kernel yields

$$\langle \phi_{(1)}^2(t) \rangle \approx Z \quad (\text{II-c-13})$$

and an approximation using the first three kernels yields

$$\langle \phi_{(3)}^2(t) \rangle \approx Z + \frac{2}{3} Z^2. \quad (\text{II-c-14})$$

If a system has random frequency modulation then the variance for a first order loop using only the first kernel is

$$\langle \phi_{(1)}^2(t) \rangle \approx \frac{p}{r(1+r)} + Qr \quad (\text{II-c-15})$$

where p is the mean square value of instantaneous frequency divided by the square of the effective bandwidth process, Q is the coherent noise-to-signal ratio in the modulation bandwidth, and r is the ratio of loop bandwidth to modulation-process bandwidth. However, this technique yields solutions which will converge only for some regions of the system inputs, and in general the technique cannot be used to predict system instabilities.

A variational formulation was used by R. D. Barnard [Ref. 22] for determining the analytic bounds of the capture range of a phase-controlled oscillator. This method divides the phase space into regions so that the system trajectories terminate in capture or noncapture domains. The capture range for a system using a simple RC filter and any form of symmetric phase comparator with normalized function $G(\phi)$ is given by

$$\xi < \inf \left\{ \lambda + K \left[\frac{\lambda^2}{K^2} + 2\lambda\phi - 2 \int_0^\infty G(Z) dZ \right]^{\frac{1}{2}} \right\} \quad (\text{II-c-16})$$

where ξ is the normalized input frequency step and λ is the largest positive value for which the quantity in the brackets has one zero in the interval $0 \leq \phi \leq 1$. The noncapture range is given by

$$\xi > \left[\frac{\pi a^2}{\alpha f_m} \int_0^1 G(Z) d(Z) \right]^{\frac{1}{2}} \quad (\text{II-c-17})$$

where a is the RC filter time constant and αf_m is the largest value of frequency shift possible in the VCO. Using the relations shown in Equations II-c-16 and II-c-17 Barnard obtained the specific inequalities that exist for both sine and sawtooth phase comparators for regular RC and lag filters.

A. J. Viterbi [Refs. 18 and 12] utilized Fokker-Planck techniques and the system model shown in Figure II-A-1 to study the effects of noise. He obtained the cumulative steady state probability distribution for a first order loop as

$$\text{Prob} (|\phi| < \phi_1) = \frac{\phi_1}{\pi} + \frac{2}{\pi} \sum_{n=1}^{\infty} \frac{I_n(\alpha) \sin n \phi_1}{n I_0(\alpha)} \quad (\text{II-c-18})$$

for $0 < \phi_1 < \pi$ and $\omega = \omega_0$. The parameter α is the signal-to-noise ratio in the bandwidth of the loop. The variance of the phase error can be shown to be

$$\sigma_{\phi}^2 = \frac{\pi^2}{3} + 4 \sum_{n=1}^{\infty} \frac{(-1)^n I_n(\alpha)}{n^2 I_0(\alpha)} . \quad (\text{II-c-19})$$

This is contrasted to the linearized model, where the variance was found to be

$$\sigma_{\phi}^2 = \frac{1}{\alpha} . \quad (\text{II-c-20})$$

For the first order loop in the general case where $\omega \neq \omega_0$ no steady state solution exists when

$$\text{SIN}^{-1} [(\omega - \omega_0)/AK] > \frac{\pi}{2} . \quad (\text{II-c-21})$$

The frequency of slipping cycles ω_s in a first order loop where $\omega = \omega_0$ and where the equilibrium phase is zero can be given by

$$\omega_s = \frac{AK}{2\pi^2 \alpha I_0^2(\alpha)} . \quad (\text{II-c-22})$$

Equation II-c-22 is an exact formula, but for large values of α it can be approximated by

$$\omega_s \approx \frac{AK \exp[-2\alpha]}{\pi} . \quad (\text{II-c-23})$$

When white Gaussian noise is applied to linear second and higher order systems, then the process is no longer Markov in that now the transition probability density function is not only a function of the present values of the process, but also of the past values. Nevertheless, it was discovered that an n^{th} order linear differential equation representing the output of an n^{th} order system driven by white Gaussian noise could be decomposed into n first-order equations in the process and its first $n - 1$ derivatives to constitute an n -dimensional vector Markov process. This in turn enabled the derivation of the n -dimensional Fokker-Planck equation. However, the solution of the partial differential Fokker-Planck equation for even the second order loop with filter $1 + a/s$

can be obtained only by very involved numerical techniques using only the stationary steady state, and even here it is not possible to determine the solution exactly, though good approximations may be made if $a \ll AK$ or for any value of a when the signal to noise ratio is large enough so that $\phi(t)$ will be small and $\sin \phi(t) \approx \phi(t)$. Then the solution for the probability-density function for the second order loop can be given by

$$p(\phi) \approx \frac{\exp [\alpha' \cos \phi]}{2\pi I_0(\alpha')} \quad (\text{II-c-24})$$

for large α' where

$$\alpha' = \frac{A^2}{4 N_0 (AK + \alpha)} \quad (\text{II-c-25})$$

A comparison was made in Ref. 18 of the various techniques available for determining the variance of the phase error for a first order loop. The linear model was a good approximation to the exact system for a signal to noise ratio of 6 db or higher, while Develet's model was good to about 2 db of signal to noise. The model of Van Trees, using Volterra functionals, was the most precise and gave excellent results down to about 1 db of signal to noise. For higher order loops the exact solution was not available to use as a reference in comparing the different techniques. However, it was found that Van Trees's model became exceedingly complex while Develet's method remained relatively simple to calculate for all loop filters and even for modulated input signals.

In Ref. 39 R. C. Tausworthe showed that the expected time of the first slipped cycle of a loop of arbitrary order satisfied a relationship which could be reduced to a linear differential equation of the first order for which formal solutions could be given. However, computation of an exact solution required the evaluation of a conditional expectation which in turn required a prior solution for the probability density of

the phase error process $p(\phi, \dot{\phi})$. Since the problem of computing $p(\phi, \dot{\phi})$ is still unsolved, an approximate evaluation of the expectation was found which was valid for loops of any order using a sine comparator. Denoting the average time to skip a cycle when starting from a particular point x_0 by $T(x_0)$, an equation was derived which held exactly for all order loops

$$T''(x_0) + g(x_0) T'(x_0) + h(x_0) = 0 \quad (\text{II-c-26})$$

where $g(x_0)$ and $h(x_0)$ are expressed in terms of conditional expectations. For a phase-locked loop with zero frequency mistuning, an open loop gain of K , and the value of the loop filter $F(s)|_{s \rightarrow \infty}$ given by F , the functions h and g may be expressed by

$$h = \frac{2}{K^2 F^2 N_0} \quad (\text{II-c-27})$$

$$g = \mu h \quad (\text{II-c-28})$$

where μ is the conditional expectation $E(\dot{\phi}_0 | \phi_0)$. Thus T is easily and exactly obtainable whenever μ can be calculated, but μ depends upon knowing $P(\phi, \dot{\phi})$ which cannot always be determined. However, the form of the solution for μ can be found, and then using a series expansion and omitting all but the first terms of the series, an approximate expression for μ may be given as

$$\mu \approx -AK F \sin \phi_0 + (AK F - \frac{\ell^2(0) \phi_0}{2 W_L} + \dots) \quad (\text{II-c-29})$$

where

$$\ell(0) = \lim_{s \rightarrow 0} s \left[\frac{AK F(s)}{s + AK F(s)} \right] \quad (\text{II-c-30})$$

and

$$W_L = AK/4 \quad (\text{II-c-31})$$

This approximation provides excellent correlation with observed experimental results.

D. SAWTOOTH PHASE COMPARATOR SYSTEMS

Sawtooth phase comparators are frequently used because of their linearity for wide ranges of phase error, which leads to improved performance for many applications. Therefore it is appropriate to consider some of the analytical techniques which apply to this system also. Several good analyses of phase-locked loops with sawtooth phase comparators are provided in Refs. 27 and 28. For a second order loop with a sawtooth comparator and a filter of

$$H(s) = \frac{1 + sT_2}{1 + sT_1} \quad (\text{II-d-1})$$

where $T_1 > T_2$, and the product of the filter, phase comparator, and oscillator gains is denoted by α , then the linear closed loop transfer function is given by

$$\frac{\theta_2(s)}{\theta_1(s)} = \frac{1 + s \frac{\tau_2}{\alpha}}{1 + \frac{2\zeta}{\omega_n} s + \left(\frac{1}{\omega_n}\right)^2 s^2} \quad (\text{II-d-2})$$

where $\tau_1 = \alpha T_1$, $\tau_2 = \alpha T_2$, and

$$\omega_n = \frac{\alpha}{\sqrt{\tau_1}} \quad (\text{II-d-3})$$

$$\zeta = \frac{1}{2} \left(\frac{\tau_2 + 1}{\sqrt{\tau_1}} \right) \quad (\text{II-d-4})$$

Equation II-d-2 is not only a linear equation, it is also an exact equation for $|\phi| < \pi$ since in the sawtooth comparator there is no need to approximate $\sin \phi$ by ϕ as the output of the phase comparator is a linear function.

The transfer ratio between input phase jitter and output phase jitter is denoted by Y and is the same as $\frac{\theta_2}{\theta_1}$ given in Equation II-d-2. With this it is now possible to compute and plot the magnitude and phase of the

jitter attenuation for various values of T_1 and T_2 as was done in Ref. 28. When the phase-locked loop is used to clean up jitter in digital signals, the noise bandwidth of Equation II-c-1 is referred to as the jitter bandwidth, and for the second order loop under consideration it is given by

$$B_j = \frac{1}{2} \pi \alpha \left(\frac{1 + \frac{\tau_2^2}{\tau_1}}{1 + \tau_2} \right) \quad . \quad (\text{II-d-5})$$

For the condition $\tau_1 = \tau_2 = 0$ which is no filter, the normalized jitter bandwidth is one half. From Equation II-d-5 it can be seen that for the sawtooth phase comparator the jitter bandwidth is independent of the input frequency mistuning. However, this is not so for the sine comparator where the jitter bandwidth can be expressed using the same notation as

$$B_j = \frac{1}{2} \cos (\phi) \left(\frac{1 + \frac{\tau_2^2}{\tau_1} \cos \phi}{1 + \tau_2 \cos \phi} \right) \pi \alpha \quad . \quad (\text{II-d-6})$$

In the sine comparator the jitter bandwidth decreases as the mistuning increases. It is also instructive to consider the interference bandwidth due to broadband noise in a sinusoidal phase comparator. The noise affects both the phase and the amplitude, and in the sinusoidal comparator the amplitude variations also affect the system output; which is in contrast to the sawtooth comparator where only the phase shift affects the output. The interference bandwidth for the sine comparator is given as

$$B_i = \frac{\alpha \pi}{2 \cos \phi} \left(\frac{1 + \frac{\tau_2^2}{\tau_1} \cos \phi}{1 + \tau_2 \cos \phi} \right) \quad (\text{II-d-7})$$

from which it can be seen that the interference bandwidth increases as the phase error increases and this causes the sinusoidal phase comparator to be more sensitive to interference than the sawtooth.

For the sawtooth comparator the time response of the phase error to a step change in input phase $\Delta\theta_1$, where the limits of the step are such that the phase error remains within $\pm\pi$ and therefore within the linear range of the response curve, is given for a second-order system by

$$\phi = \Delta\theta_1 \exp[-\zeta\omega_n t] \left\{ \cosh [\sqrt{\zeta^2-1}(\omega_n t)] - \frac{\zeta - \frac{\omega_n}{\alpha}}{\sqrt{\zeta^2-1}} \sinh [\sqrt{\zeta^2-1}(\omega_n t)] \right\}. \quad (\text{II-d-8})$$

For a step change in input frequency $\Delta\omega_i$, the phase error as a function of time is given by

$$\phi = \frac{\Delta\omega_i}{\alpha} \left\{ 1 - \exp[-\zeta\omega_n t] \left[\cosh (\omega_n t \sqrt{\zeta^2-1}) - \frac{\frac{\alpha}{\omega_n} - \zeta}{\sqrt{\zeta^2-1}} \sinh (\omega_n t \sqrt{\zeta^2-1}) \right] \right\}. \quad (\text{II-d-9})$$

All the formulations given so far for the sawtooth comparator have been based on the small signal case where $|\phi| < \pi$ and in this region the system is perfectly linear and therefore all the above results are exact. The results also hold exactly even when there is an initial frequency mistuning, so long as the frequency difference is less than the seize frequency, which is the maximum mistuning of a suddenly connected signal which will not cause skipped cycles. For the sawtooth comparator the seize frequency is given by

$$\omega_s = \left(\frac{\tau_2}{\tau_1} \right) \pi \alpha, \quad (\text{II-d-10})$$

while for the sine comparator it is found to be only [Ref. 8]

$$\omega_s = \alpha \left(\frac{\tau_2}{\tau_1} \right) \quad (\text{II-d-11})$$

which is a factor of π less than that for the sawtooth comparator.

For large initial frequency differences there is a critical frequency called the pull-in frequency where the asynchronous flicker mode disappears and the system must eventually reach a synchronous condition since there exists no asynchronous solution. A. J. Goldstein [Ref. 27] has found an exact answer for the pull-in frequency as

$$\omega_p = \Pi\alpha \left\{ \frac{1 - D}{\tanh \frac{1}{2} \zeta \omega_n T_0} + D \tanh \frac{1}{2} \zeta \omega_n T_0 \right\} \quad (\text{II-d-12})$$

where T_0 , the critical flicker period, is the smallest positive solution of

$$\sqrt{\zeta^2 - 1} \left(\frac{\tanh \frac{1}{2} \zeta \omega_n T_0}{\tanh \frac{1}{2} \sqrt{\zeta^2 - 1} (\omega_n T_0)} \right) = \sqrt{\tau_1} \zeta - \frac{\tau_1}{\tau_2} \left(1 - \sqrt{1 - \frac{\tau_2}{\tau_1}} \right) = C_1 \quad (\text{II-d-13})$$

and D is given by

$$D = \frac{C_1 (\zeta \sqrt{\tau_1} - 1) - \tau_1 (\zeta^2 - 1)}{C_1^2 - \tau_1 (\zeta^2 - 1)} \quad (\text{II-d-14})$$

Computer solutions to Equation II-d-12 are plotted in Ref. 28. For $\tau_2 \gg 1$ and $\frac{\tau_2}{\tau_1} < 0.5$ the pull-in frequency approaches

$$\omega_p \approx \frac{2\Pi\alpha}{\sqrt{3}} \sqrt{\frac{\tau_2}{\tau_1}} \quad (\text{II-d-15})$$

The pull-in frequency of the sawtooth and sinusoidal phase comparators is plotted in Ref. 28 and, for the cases considered, the pull-in range of the sawtooth is at least double that for the sinusoidal comparator.

The time required for a suddenly applied signal to lock may be calculated for the sawtooth comparator subject to the assumption that the voltage to the VCO does not change except at the time of the applied sample results. The formula is

$$T_{\text{LOCK}} = T_2 \int_{\frac{\omega_m}{\omega_L}}^{\frac{\tau_2}{\tau_1}} \frac{\frac{\tau_1}{\tau_2}}{\frac{\omega_m}{\omega_L} - \left(\frac{\tau_1}{\tau_2} \frac{\omega_I}{\omega_L} \right) + \left(1 - \frac{\tau_2}{\tau_1} \right) \left[\coth^{-1} \left(\frac{\tau_1}{\tau_2} \frac{\omega_I}{\omega_L} \right) \right]^{-1}} d\left(\frac{\omega_I}{\omega_L} \right) \quad (\text{II-d-16})$$

where ω_I is the instantaneous mistuning parameter introduced by D. Richman [Ref 8], ω_m is the mistuning frequency, and ω_L is the lock frequency. However, Equation II-d-16 does not consider the effects of variations in the initial phase.

A somewhat different approach was used by F. G. Splitt [Ref. 55] to analyze a sawtooth phase-locked loop over a wide dynamic range. It was observed that since the system was linear for $|\phi| < \pi$ and that an exact solution could be given, starting with an arbitrary set of initial conditions, for ϕ within the linear limits. If, when ϕ reached the limits of the linear region, the equations were solved for all system values, these values could then be used as the starting point for a new interval of $-\pi < \phi < \pi$. In this way an exact solution could be found within each interval and the process could be repeated until the conditions at the end of one interval were such as to permit pull-in during the next interval. The total pull-in time could then be found exactly by adding up the times spent in each interval.

For a second order system with a filter transfer function of $a + b/s$, the characteristic equation of the system can be expressed in terms of ζ and ω_n and then further substitutions made by letting

$$\alpha = \zeta^{-1} \sqrt{1 - \zeta^2} \quad (\text{II-d-17})$$

$$\beta = \omega_n \sqrt{1 - \zeta^2} \quad . \quad (\text{II-d-18})$$

The system solution for $-\pi \leq \phi < \pi$ is then given by

$$\phi(t) = \frac{1}{\alpha} \exp\left[-\frac{\beta t}{\alpha}\right] [(y_0 - \phi_0) \sin \beta t + \alpha \phi_0 \cos \beta t] \quad (\text{II-d-19})$$

where y_0 is the normalized initial frequency offset and ϕ_0 is the initial phase offset. If the phase offset is held fixed, it is possible to determine the minimum value of y_0 (denoted by \hat{y}_0) which maintains the

solution in the range $|\phi| < \pi$ by solving for the extreme values of $\phi(t)$ and determining the point where the extreme equals $\pm \pi$. The relation between y_0 and ϕ_0 which keeps the system from skipping any cycles is given by

$$\pi = A \exp \left[-\frac{1}{\alpha} \tan^{-1} \alpha \right] \begin{cases} \cdot \exp [-\theta] & \text{if } -\pi \leq \phi_0 < 0 \\ \cdot \exp [\theta] & \text{if } 0 \leq \phi_0 < \pi \end{cases} \quad (\text{II-d-20})$$

where

$$A = |\phi_0| \sqrt{\left[\left(1 - \frac{y_0}{\phi_0} \right)^2 + \alpha^2 \right] / (1 - \alpha^2)} \quad (\text{II-d-21})$$

and

$$\theta = \frac{1}{\alpha} \tan^{-1} \left| \frac{\alpha \phi_0}{y_0 - \phi_0} \right| \quad (\text{II-d-22})$$

From Equation II-d-20 it is found that the minimum value of \hat{y}_0 occurs when $\phi_0 = \pi$ and the maximum value of \hat{y}_0 is when $\phi_0 = 0$. A complete curve of \hat{y}_0 as a function of ϕ_0 for various values of ζ is given in Ref. 55.

It has also been shown that when y_0 is greater than \hat{y}_0 , there is a decrease in frequency during each cycle of ϕ so that the mistuning frequency is always less at the end of a cycle than at the beginning of the cycle. This indicates that the system has a theoretically infinite lock range in the absence of noise.

The pull-in time for the phase error to come within $\frac{\pi}{10}$ of the steady state value during the lock cycle is given by the largest value of τ_p which satisfies

$$\frac{\pi}{10} = \exp[-\tau_p] \begin{cases} \cdot [\phi_0 + (y_0 - \phi_0)\tau_p] & \text{for } \zeta = 1 \\ \cdot \left[\frac{1}{\alpha} \sqrt{(y - \phi_0)^2 + (\alpha\phi_0)^2} \right] \left| \sin(\alpha\tau_p + \psi) \right| & \text{for } 0 \leq \zeta < 1 \end{cases} \quad (\text{II-d-23})$$

$$\text{where } \psi = \begin{cases} \tan^{-1} \frac{\alpha \phi_0}{(y_0 - \phi_0)} & \text{for } \frac{y_0}{\phi_0} \geq 1 \\ \pi - \tan^{-1} \left| \frac{\alpha \phi_0}{(y_0 - \phi_0)} \right| & \text{for } \frac{y_0}{\phi_0} < 1 \end{cases} \quad (\text{II-d-24})$$

The time for the system to pass through the i^{th} cycle while proceeding towards lock can be approximated by

$$\tau_i = \frac{2}{\alpha} \tan^{-1} \alpha \left[\frac{y_i}{\pi} + 1 \right]^{-1} \quad (\text{II-d-25})$$

where y_i is the normalized frequency offset at the beginning of a cycle.

The total time to pull-in is then given by

$$T_p = \tau_{N+1} + \sum_{i=1}^N \tau_i \quad (\text{II-d-26})$$

which is the time spent passing through each of the N cycles required to get within single cycle pull-in range plus the time spent in the last cycle.

An exact graphical method of evaluating the number of skipped cycles and the pull-in time for a second order phase-locked loop with a sawtooth comparator was given by E. N. Protonotarios in Ref. 29. However, this method relied heavily on phase-plane techniques and therefore it is not very effective for third and higher order systems.

E. MODIFICATIONS OF THE LOOP FILTER

All the systems analyses considered so far have assumed that the loop filter was a continuous linear filter, and variations to the system dynamics were accomplished by changing the transfer function of the linear filter or by modifying the phase comparator. However, modifications to the actual structure of the filter provide additional possible means of improving the phase-locked loop's performance for particular applications.

The deliberate introduction of non linearities into the loop filter was studied by B. J. Leon and L. L. Cleland in Ref. 33. It was noted that any filter of the form

$$F(s) = K_1 \left(A_0 + \frac{A_1}{s} + \frac{A_2}{s^2} \dots \frac{A_n}{s^n} \right) \quad (\text{II-e-1})$$

could be expressed by

$$e_o = K_1 \left\{ A_0 x(t) + A_1 \int_0^t x(t_1) dt_1 + A_2 \int_0^t \int_0^{t_1} x(t_2) dt_2 dt_1 \dots \right. \\ \left. A_n \int_0^t \int_0^{t_1} \dots \int_0^{t_{n-1}} x(t_n) dt_n dt_{n-1} \dots dt_1 \right\} \quad , \quad (\text{II-e-2})$$

and that the performance of this filter could be significantly changed if the constant gains $A_0, A_1, A_2, \dots A_n$ were replaced by nonlinear functions $A_0(x), A_1(x), A_2(x), \dots A_n(x)$. The problem is to find the proper nonlinear gains $A_i(x)$ so that the system has the small signal characteristics of the original system and yet possesses the desired extended lock and tracking ranges. Finding the nonlinear gains can be very difficult unless all the $A_i(x)$ have the same form, in which case the nonlinear portion can be factored out and combined with K_1 . Then it is further possible to combine the nonlinearity of the phase comparator with the nonlinearity of the filter, which can be accomplished graphically. The actual design procedure is relatively simple; first the desired overall characteristics of the system are determined based upon required performance criterion, then since the nonlinear features of the phase comparator are known it is possible to determine graphically or analytically by computer program the shape of the nonlinear filter characteristics which will be needed to give the overall result. Thus improved performance has been gained, but at the expense of a more complex circuit.

Currently there exists strong trends towards digital forms of the phase-locked loop, and although all portions of the loop including the VCO have been digitized for specific applications, the only technique expanded upon in this section will be that of digitizing the loop filter.

A technique was developed by S. C. Gupta [Ref. 47] for design of an optimum digital filter for analog-digital phase locked loops. In this method continuous input and VCO signals were used with a sampler located between the phase comparator and the filter, and a zero-order hold circuit placed between the filter and the VCO. The filter was designed by minimizing the sum of the integral squared value of the output noise of the VCO due to the input noise and the squared value of the sampled error between the actual phase input and the output phase of the VCO. The optimum discrete filter characteristics were found to be

$$D(Z) = \frac{\omega_o(Z)}{1 - \omega_o(Z)G(Z)} \quad (\text{II-e-3})$$

where $G(Z)$ is the transfer function of the zero order hold circuit with the VCO and $\omega_o(Z)$ is given by

$$\omega_o(Z) = \frac{Z \left[\frac{\lambda G(Z^{-1}) \theta(Z^{-1}) \theta(Z)}{Z P^-(Z)} \right]}{P^+(Z)} \quad (\text{II-e-4})$$

where

$$P(Z) = P^+(Z) P^-(Z) = NT \int_0^T G(Z, m) G(Z^{-1}, m) dm + \lambda G(Z) G(Z^{-1}) \theta(Z^{-1}) \theta(Z), \quad (\text{II-e-5})$$

$\theta(Z)$ is the input phase, $P^+(Z)$ represents the poles and zeroes inside the unit circle, $P^-(Z)$ represents the poles and zeroes outside the unit circle, and λ is a factor determined by the selected value of noise bandwidth.

Using these formulas, the exact expression for the filters of systems subjected to step inputs of phase and also for ramp changes in phase have been derived in Ref. 47. In comparison to the continuous loop filter, it was found that the optimum digital filter was one degree higher than that of a continuous system.

While the material presented may neither be completely comprehensive, nor does it include many steps of the original derivations, yet the overall sequel should provide a good understanding of the basic analytical techniques available in the design and analysis of phase-locked loop systems.

III. EXPERIMENTAL INVESTIGATION OF A THIRD ORDER TYPE TWO SYSTEM

A. THE SPECIFIC PROBLEM

In an effort to extend the reservoir of information available on phase-locked loop systems, the particular configuration selected for detailed theoretical and experimental research was one which had not previously been developed in detail in the literature. A third order system was chosen because it had been indicated that the tracking behavior of a loop initially in lock could be extended by increasing the order of the loop from second to third [Ref. 12], and there was also some evidence to indicate that improved acquisition time might be obtained with a third order system [Ref. 41]. Then there was the practical aspect that if the characteristics of third order systems were better known and understood, designers might begin to utilize it in particular applications and realize improved performance over first or second order loops. The third order configuration was pursued in spite of the reservations expressed by some of the authoritative writers on the subject indicating that third order loops might experience stability problems and that there was little need for any system of higher than second order.

The type number of the system investigated was selected to be Type Two for several reasons. The first reason was the fact that very little previous work has been done on Type Two phase-locked loop systems, and the second reason was that with a Type 2 system the application of linear servomechanism theory indicated that there should be zero steady state phase error for a step input of frequency or phase. The specific way in which this third order Type Two system was formulated is discussed below.

1. Normalization of System Parameters

In order to enable the results of this study to be easily interpreted and applied to any operating condition, all circuit parameters have been normalized. The normalization procedure selected can easily be understood with the aid of Figure III-A-1 which shows a sketch

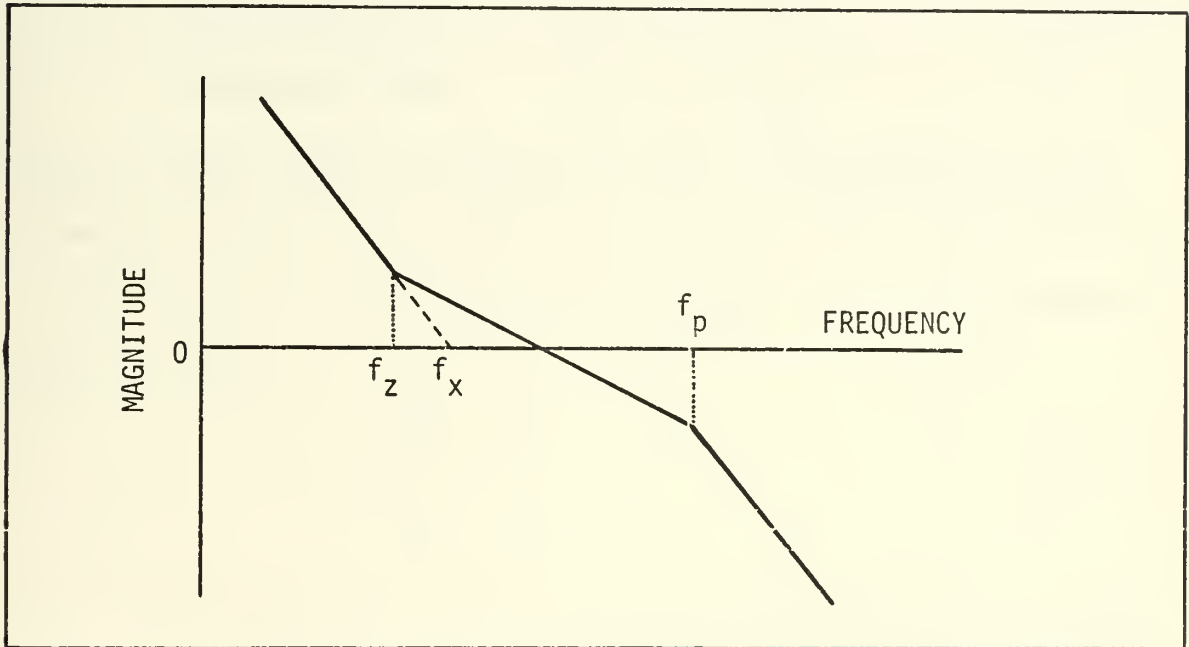


Figure III-A-1. Open-Loop Bode Magnitude Curve for a Type 2 Third-Order System.

of the typical open loop Bode magnitude curve for a Type 2 third order system with a transfer function of

$$GH = \frac{(f_x)^2 \left(\frac{s}{f_z} + 1 \right)}{s^2 \left(\frac{s}{f_p} + 1 \right)} \quad . \quad (III-a-1)$$

The gain of this system is given as the square of the frequency f_x which is the extended zero axis intercept of the low frequency magnitude curve.

Since the center operating frequency of the phase-locked loop, which is also the VCO free running frequency f_{VCO} , is the most distinguishing parameter of the circuit, this frequency shall be used

as the basis of the system normalization. The normalized parameters are then expressed as:

$$\text{Normalized frequency} = f_n = f/f_{vco} \quad (\text{III-a-2})$$

$$\text{Normalized Zero} = a_n = f_z/f_{vco} \quad (\text{III-a-3})$$

$$\text{Normalized Pole} = b_n = f_p/f_{vco} \quad (\text{III-a-4})$$

$$\text{Normalized Time} = t_n = t(f_{vco}) \quad (\text{III-a-5})$$

$$\text{Normalized Gain} = k_n = (f_x/f_{vco})^2 . \quad (\text{III-a-6})$$

Using the above normalized factors the entire system operation can be described in terms of the normalized frequency and the normalized time, with the open loop transfer function of Equation III-a-1 now expressed in normalized form as

$$GH = \frac{k_n \left(\frac{s}{a_n} + 1 \right)}{s^2 \left(\frac{s}{b_n} + 1 \right)} . \quad (\text{III-a-7})$$

The inverse transformation from normalized parameters to actual system parameters can be accomplished using the following relationships:

$$f = f_{vco} f_n \quad (\text{III-a-8})$$

$$f_z = f_{vco} a_n \quad (\text{III-a-9})$$

$$f_p = f_{vco} b_n \quad (\text{III-a-10})$$

$$\text{gain} = k_n (f_{vco})^2 \quad (\text{III-a-11})$$

$$t = t_n / f_{vco} . \quad (\text{III-a-12})$$

The use of the above normalization procedures allows an easy conversion to be made between the normalized results presented in this treatise and any desired operating conditions.

2. Composition of Signal Waveforms

For this particular study the input signal waveform and the VCO output waveform both consisted of pulse trains made up of very short

duration pulses. These waveforms were used because the original application which generated the motivation for this thesis was concerned with the use of a phase-locked loop to synchronize digital data transmissions in computer systems. The use of pulse waveforms does not seriously limit the applicability of the results, since pulsed outputs are easily obtained from sinusoidal signals or any type of periodic waveform by detection of zero crossovers or other elementary pulse forming techniques. In fact, as will be shown later, sinusoidal oscillators were actually used in the simulation process of this research work and then their output modified to obtain the desired pulsed waveforms.

In order to allow convenient simulation and presentation of results using the Naval Postgraduate School's hybrid computer system, the VCO signal was normalized to a free running frequency of one Hertz. This normalization also allowed simplified frequency scaling so that the results could be applied to any desired frequency range.

3. Phase Comparator

The operating characteristics of the phase comparator used in the basic simulation program is depicted in Figure III-A-2. The output of

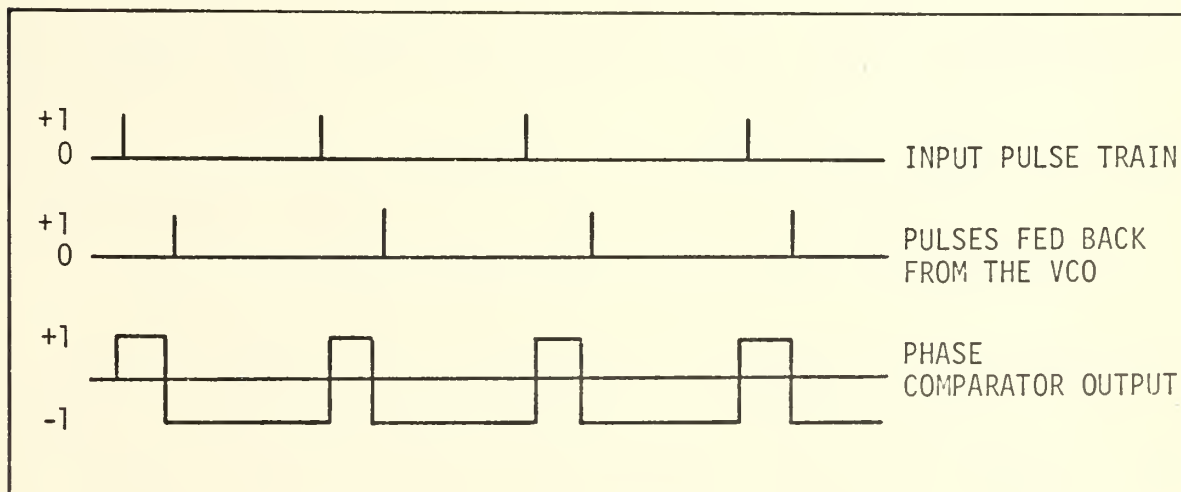


Figure III-A-2. Phase Comparator Operating Characteristics.

III-A-4 shows the output as a function of phase error for a sinusoidal and a sawtooth phase comparator whose gains have been adjusted so that their outputs are equal for small values of phase error. It can be seen

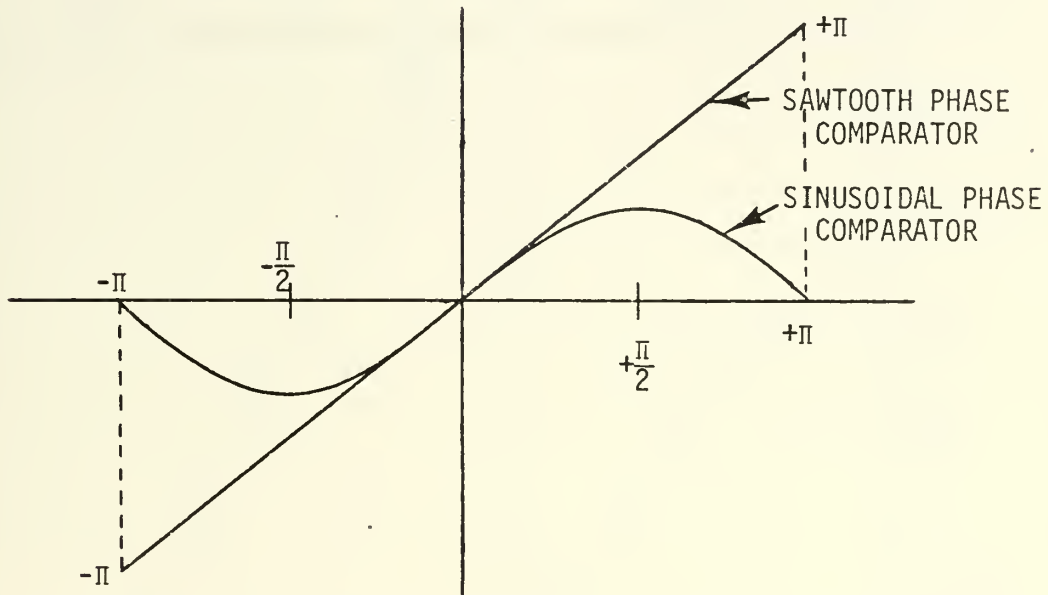


Figure III-A-4. Comparison of the Sinusoidal and Sawtooth Phase Comparator Operating Characteristics.

that for phase errors in excess of $\frac{\pi}{2}$ radians the sawtooth phase comparator's output is much greater than that of the sine comparator and thus a greater control voltage is applied to the VCO when it is most needed to help acquire or maintain phase lock.

4. Loop Filter

For a Type 2 system such as that under investigation, the phase margin is zero at the gain cross over; therefore, phase-lead compensation must be introduced into the system to give a positive phase margin and proper system damping. The gain of the system was originally selected on the basis of bandwidth and settling time considerations, and then phase-lead compensation was applied. The Bode plot of the compensated open-loop transfer function used in the basic simulation is shown in Figure III-A-5, and the normalized transfer function is given by

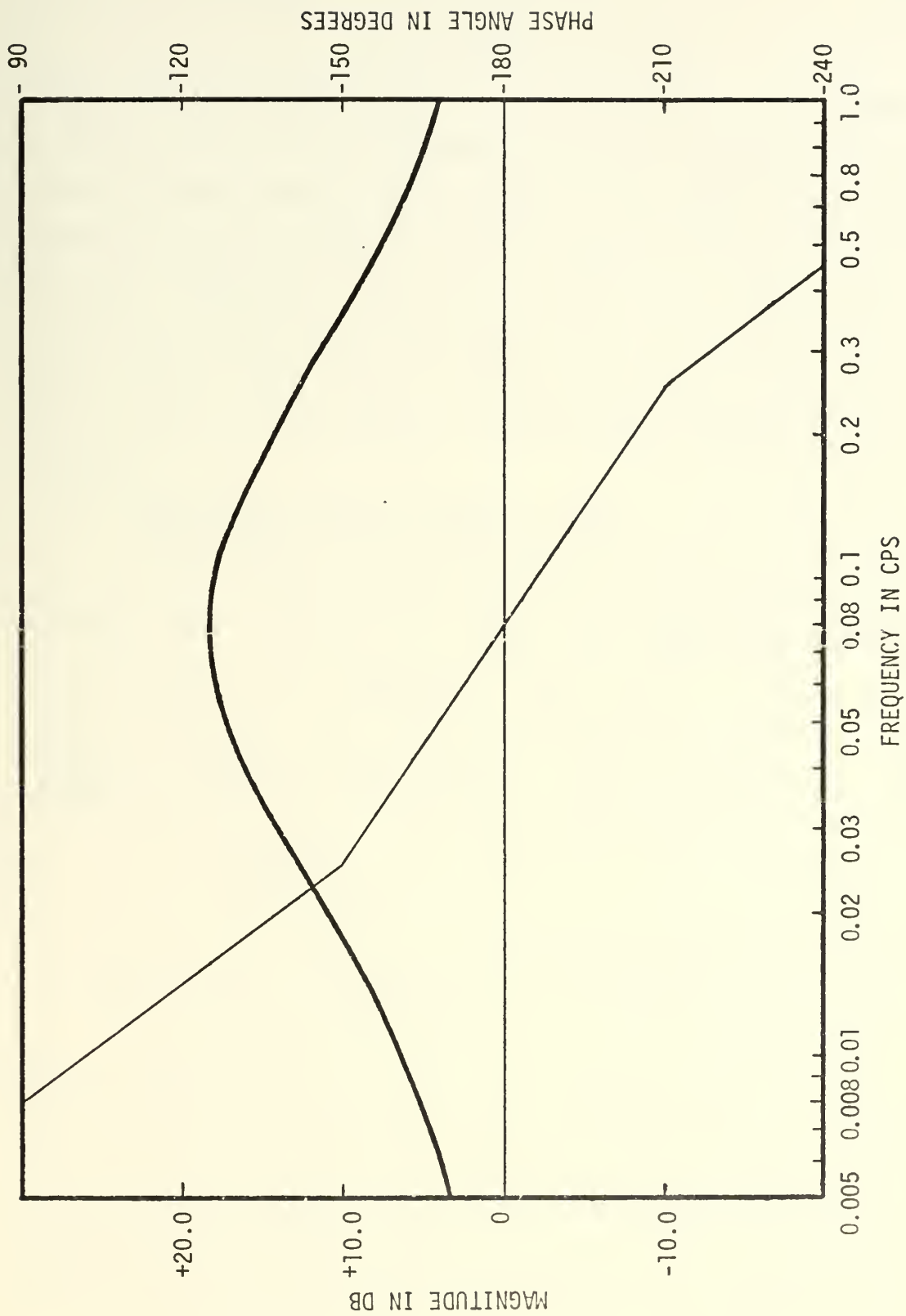


Figure III-A-5. Bode Plot of Open Loop Transfer Function.

$$G(jf) = \frac{0.002 \left(\frac{jf}{0.025} + 1 \right)}{(jf)^2 \left(\frac{jf}{0.25} + 1 \right)} . \quad (\text{III-a-13})$$

From Figure III-A-5 it is seen that the phase margin is 55 degrees, and a Nichols chart plot of the transfer function of Figure III-A-5 showed that the closed-loop-system bandwidth was 0.132 Hertz. Note that both the Bode diagram of Figure III-A-5 and Equation III-a-13 are expressed in terms of frequency in Hertz rather than in radians per second. The use of Hertz, together with the normalized simulation frequency of one Hertz, allows easy conversion of the experimental results to any desired frequency.

5. Block Diagram of the Complete System

The components described above were combined as shown in Figure III-A-6 to give a complete third order Type 2 phase-locked system. The

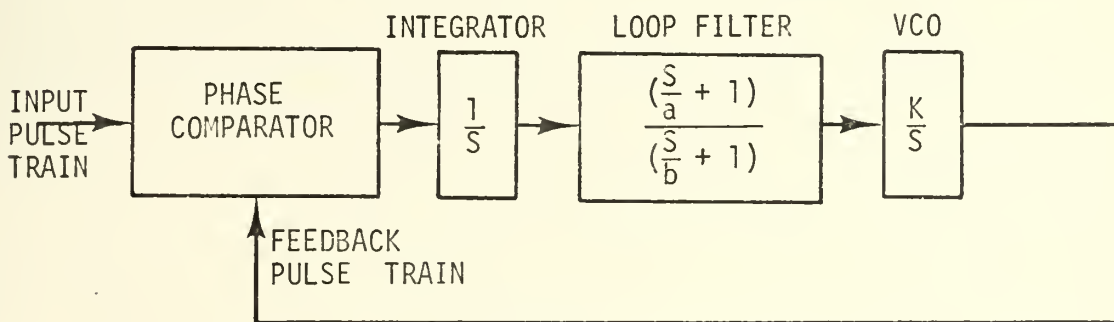


Figure III-A-6. Block Diagram of the Third Order Type 2 Phase-Locked System.

VCO has been represented by K/S where K incorporates all the loop gains and has the units of cycles per second per volt, thus converting the input voltage to a frequency; and the $1/S$ represents the integration of frequency to give the final output of the VCO which is phase. This system was the starting point of the simulation study whose objective

was to investigate the effects of the various components on the overall system performance.

B. ANALOG SIMULATION

The majority of experimental work for this thesis was accomplished using a Comcor Inc. CI-5000 analog computer which has both an analog section and a digital patchable logic section. Some utilization was made of a hybrid configuration by interconnecting the analog computer and a Scientific Data Systems SDS-9300 digital computer. In the hybrid configuration the digital computer was used primarily to control the program operations and to accomplish measurements on the system. Some of the difficulties encountered in the hybrid simulation were concerned with the precision and the stability of the system's components. The CI-5000 analog computer was designed to have a precision of 0.01 per cent, and tests indicated that this degree of precision actually existed in the equipment used; however, for certain aspects of the simulation, improved precision and stability might have been advantageous.

In the remainder of this section a brief description will be given of the techniques used to simulate the operation of the basic phase-locked loop system described in Subsection A.

1. Input Signal Generator

Several simulation techniques were available to generate the required input pulse train. The method selected is shown in Figure III-B-1 and was singled out because it was the most stable at the required operating frequency, yielding an average of 0.015 per cent variation in period duration as measured by the digital computer using a 100 kc clock. The delay flip-flop was reset automatically at the start of each new problem run by a signal from the compute mode control.

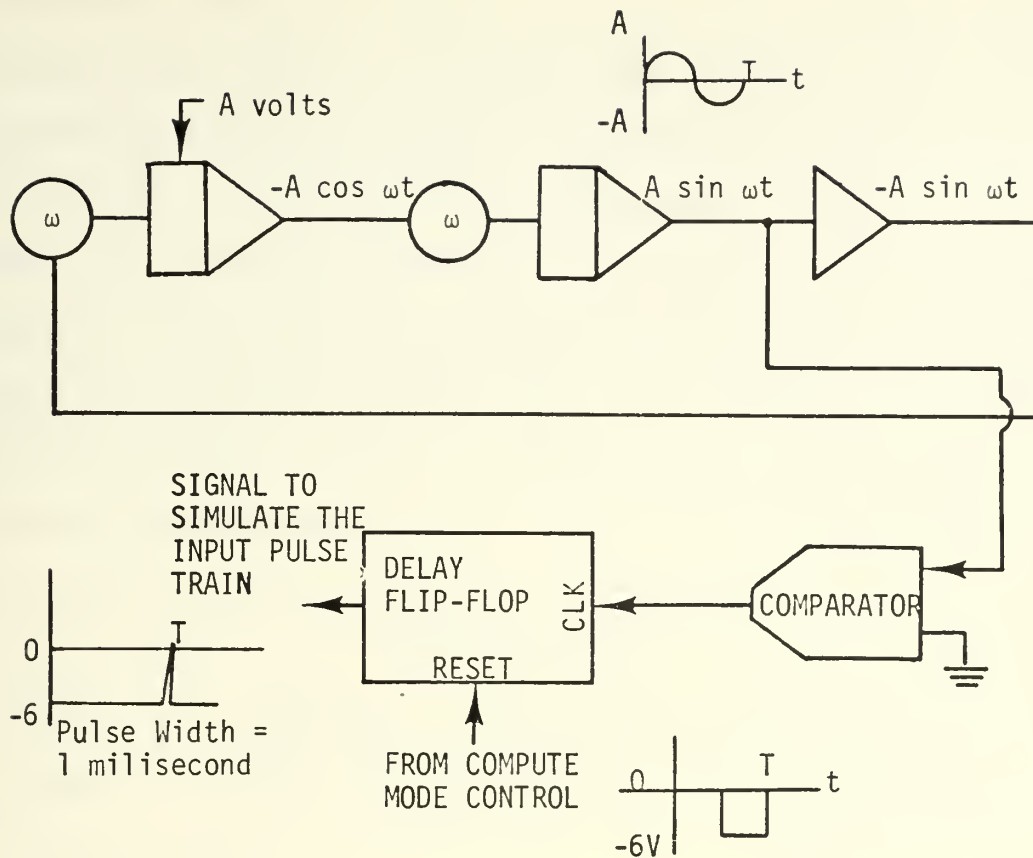


Figure III-B-1. Analog Circuit Used to Simulate the Input Pulse Train.

This insured that the starting phase of the input signal was always zero for each run. The waveforms generated throughout the system are also shown in Figure III-B-1 at their respective locations. The displacement of the output from the zero axis is explained by noting that all outputs from the logic components of the CI-5000 computer must be either 0 or -6 volts.

2. VCO

The VCO selected for use in the simulation was that given by C. L. Johnson in Ref. 56. It was found that direct application of the circuit at a frequency of one hertz did not give the desired stability and linearity of operating characteristics, therefore the frequency of operation was adjusted until an operating point was found where the

system had a stability of about 0.015 per cent and the output frequency was relatively linear for a sufficiently wide range of input voltage. It was then necessary to reduce the frequency of the VCO by a factor of 13 to obtain the required one hertz free running frequency. The frequency reduction was accomplished on the logic portion of the analog computer by using a binary-coded-decimal (BCD) counter to generate a single output for each 13 input pulses. The diagram of the complete VCO including countdown circuits is shown in Figure III-B-2 together with the associated waveforms.

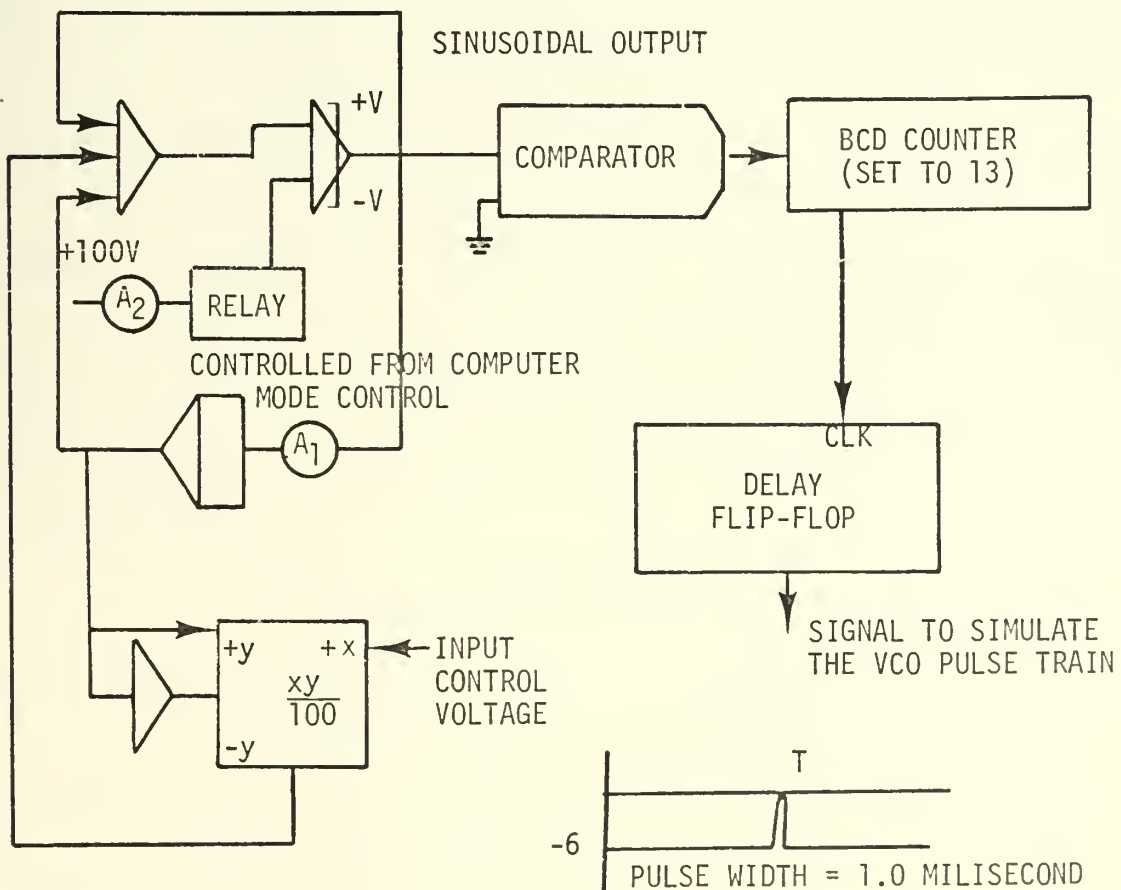


Figure III-B-2. Analog Circuit Used to Simulate the VCO.

One modification to the VCO used in this simulation as compared to the VCO described by Johnson was the addition of a relay switching

circuit to the input of the limiter amplifier. This circuit applied a positive voltage to insure that the amplifier was saturated with the same polarity at the start of each run. In addition, the BCD reset was slaved to the main computer mode control so that at the start of each run the counter would be reset to a specified counter setting. In this way the initial phase of the VCO with respect to the input oscillator could easily be set to any of 13 discrete increments, each separated by about 27.69 degrees.

Any further reference to the VCO in the remainder of this treatise shall imply reference to the entire circuit of Figure III-C-2 including oscillator and frequency divider circuits as a single integral circuit with a free-running frequency of one hertz.

The output frequency as a function of input voltage for the VCO system is shown plotted in Figure III-B-3. It is seen that the response curve may be approximated by a straight line for small values of input voltages, and the slope of this line determines the gain of the VCO in hertz per volt. For the central portion of the curve the gain has been computed to be

$$\text{Gain}_{\text{VCO}} = 0.0046 \text{ hertz/volt} \quad . \quad (\text{III-b-1})$$

3. Phase Comparator

The basic component of the phase comparator is a reset-set (RS) flip-flop with the input pulse train applied to the set terminal and the pulse train from the VCO applied to the reset terminal. Thus the flip-flop is turned on by the input pulse and turned off by the VCO pulse. Figure III-B-4 shows the circuit diagram of the phase comparator together with the waveforms which are generated at the output of each major component. The digital/analog switches serve to convert the logic

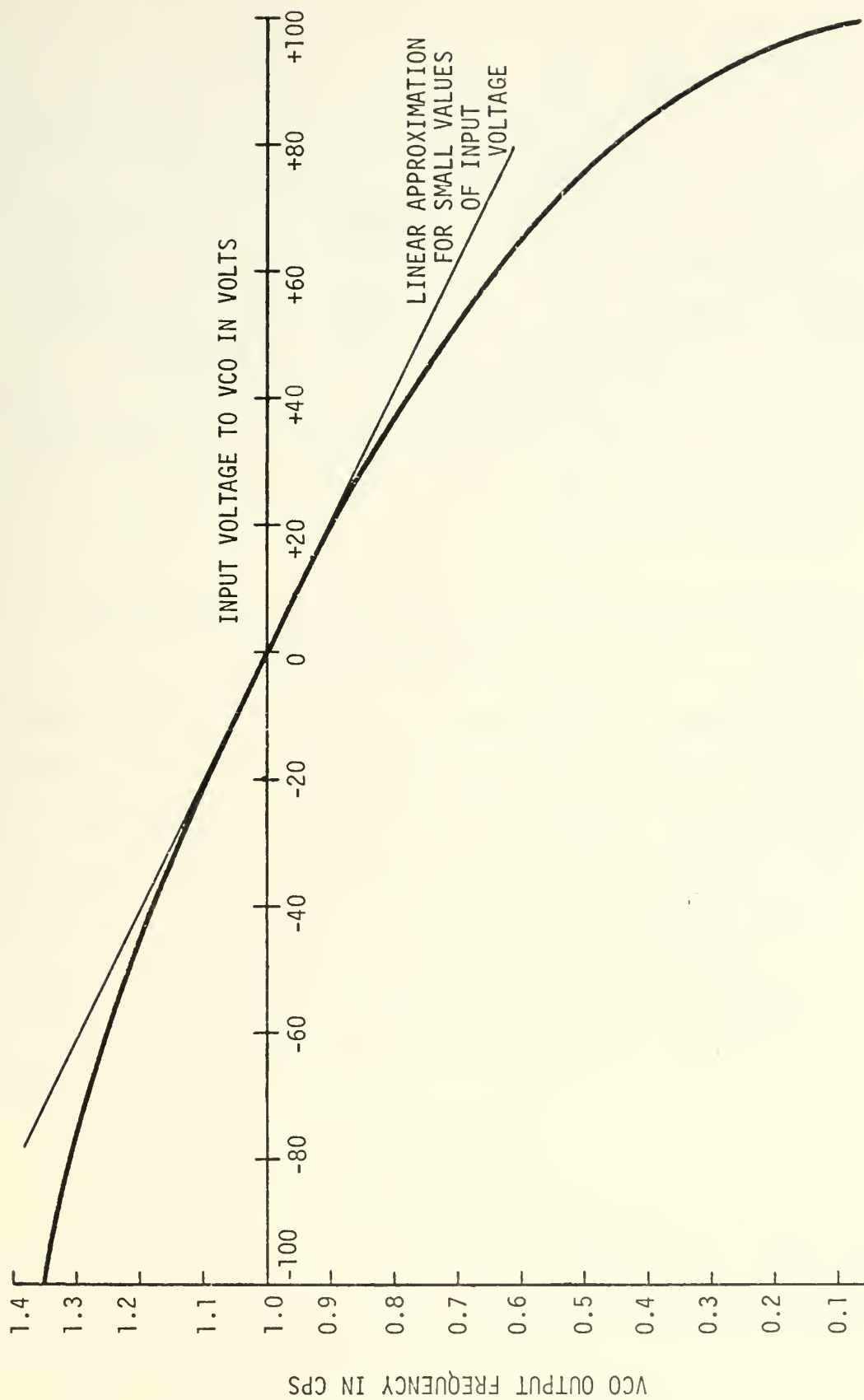


Figure III-B-3. Output Frequency of the VCO as a Function of Input Frequency.

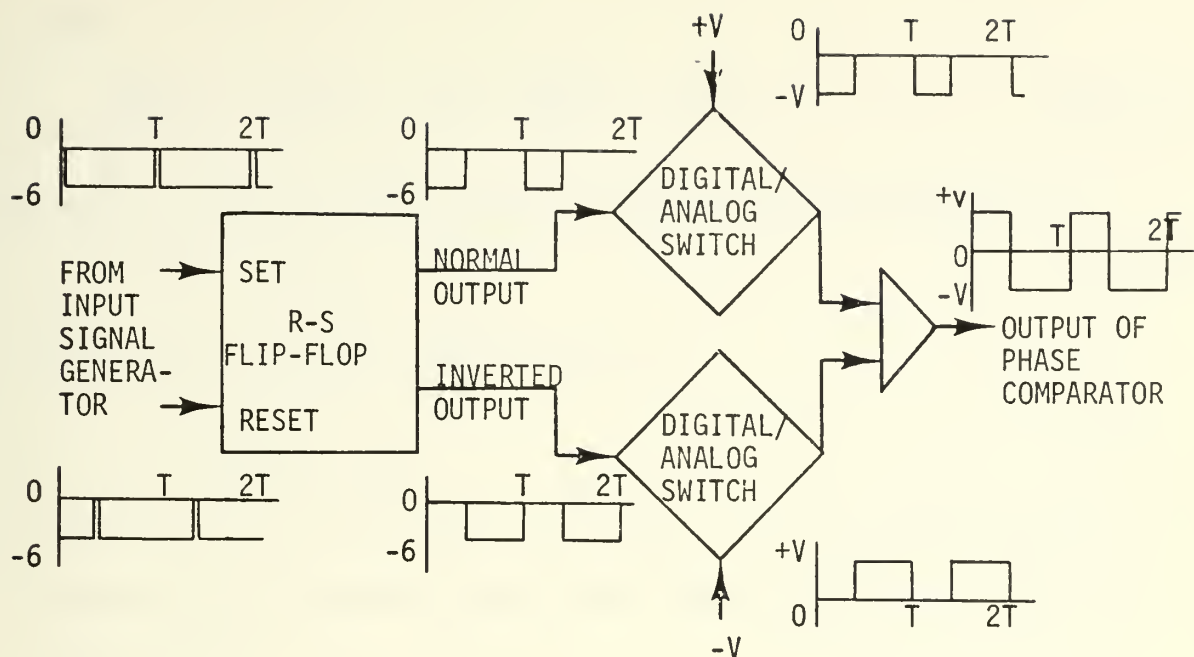


Figure III-B-4. Analog Circuit Used to Simulate the Sawtooth Phase Comparator.

signals into the required voltage waveforms to be applied to the loop filter, and in the CI-5000 these switches incorporate a sign inversion. The gain characteristics of the phase comparator, which correspond to the slope of the sawtooth function shown in Figure III-A-3, can be increased or decreased in direct proportion to the value of the voltage V applied to the digital/analog switches. In this simulation V was set at 10 volts, giving the phase comparator a gain factor of $10/\pi$ volts per radian.

4. Filter

From Figure III-A-6 it was seen that the loop filter consisted of an integrator and one section of lead-lag compensation. The integration can be simulated directly and the transfer function of the lead-lag compensator can be expressed as

$$\frac{E_o(s)}{E_{in}(s)} = \frac{(s/a + 1)}{(s/b + 1)} = \frac{Z(s)}{E_{in}(s)} \frac{E_o(s)}{Z(s)} \quad (\text{III-b-2})$$

where

$$\frac{Z(s)}{E_{in}(s)} = \frac{1}{(s/b + 1)} \quad \text{AND} \quad \frac{E_o(s)}{Z(s)} = s/a + 1 . \quad (\text{III-b-3})$$

The first relationship of Equation III-b-3 can be rearranged as

$$s Z(s) = b[E_{in}(s) - Z(s)] \quad (\text{III-b-4})$$

and solved in the time domain yielding

$$z = b \int (e_{in} - z) dt \quad (\text{III-b-5})$$

Equation III-b-4 can then be substituted into the second relationship of Equation III-b-3 and the system simplified and converted into the time domain to give

$$e_o = \left(\frac{b}{a}\right) e_{in} - z \left(\frac{b}{a} - 1\right) . \quad (\text{III-b-6})$$

The analog solution of Equations III-b-5 and 6 for the condition $a = 0.025$ and $b = 0.25$ is shown below in that portion of Figure III-B-5 which is marked lead-lag compensator. The integrator and amplifier

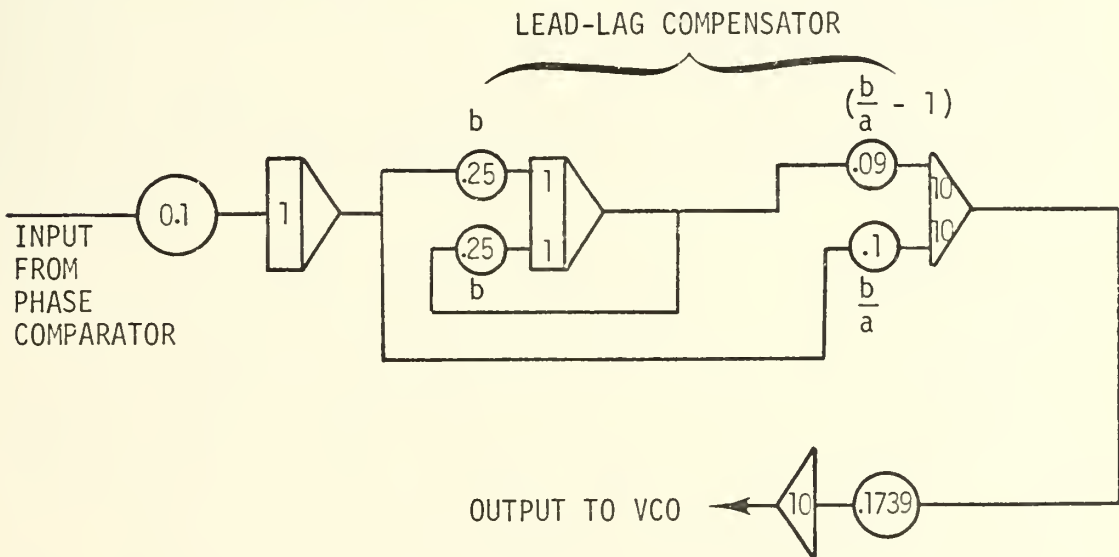


Figure III-B-5. Analog Circuit Used to Simulate the Loop Filter.

making up the lead-lag compensator have an overall gain of 0.1. The remainder of the loop filter shown in Figure III-B-5 consists of an

integrator prior to the compensation network which is required to make the loop a third order system, and the necessary amplifiers and potentiometers following the compensator to make the total loop gain correspond to the value of 0.002 which was specified by the Bode diagram of Figure III-A-5 for the initial simulation problem.

5. Complete Analog Program

The complete program as set up on a CI-5000 analog computer is shown in Figure III-B-6. For easy reference the diagram includes actual connection points from which signals are taken for recording on the Brush Instruments, Mark 200 8 channel recorder. A tabulation of the loop gain can be made from Figure III-B-6 as follows:

<u>COMPONENT</u>	<u>GAIN</u>
Phase comparator	$10/\pi$ volts/radian
Integrator and its potentiometer	0.1
Lead-lag compensator	0.1
Amplifiers and potentiometers following compensator	2.174
VCO	$0.0046(2\pi)$ radians/sec-volt

The total loop gain is the product of the component gains listed above and is 0.002, which concurs with the gain specified for the initial simulation.

The output of a typical simulation run is shown in Figure III-B-7 to assist in describing the system's operation. This figure shows the waveforms which were generated at the critical points throughout the circuit for the particular initial conditions where the input frequency was 1.02 hertz or 2.0 percent higher than the VCO free-running frequency, and the VCO signal lagged the input signal by 360 degrees which is 180 degrees from the steady state lock condition. For proper operation of the circuit the pulsed waveforms shown on channels 3 and 4 of Figure III-B-7

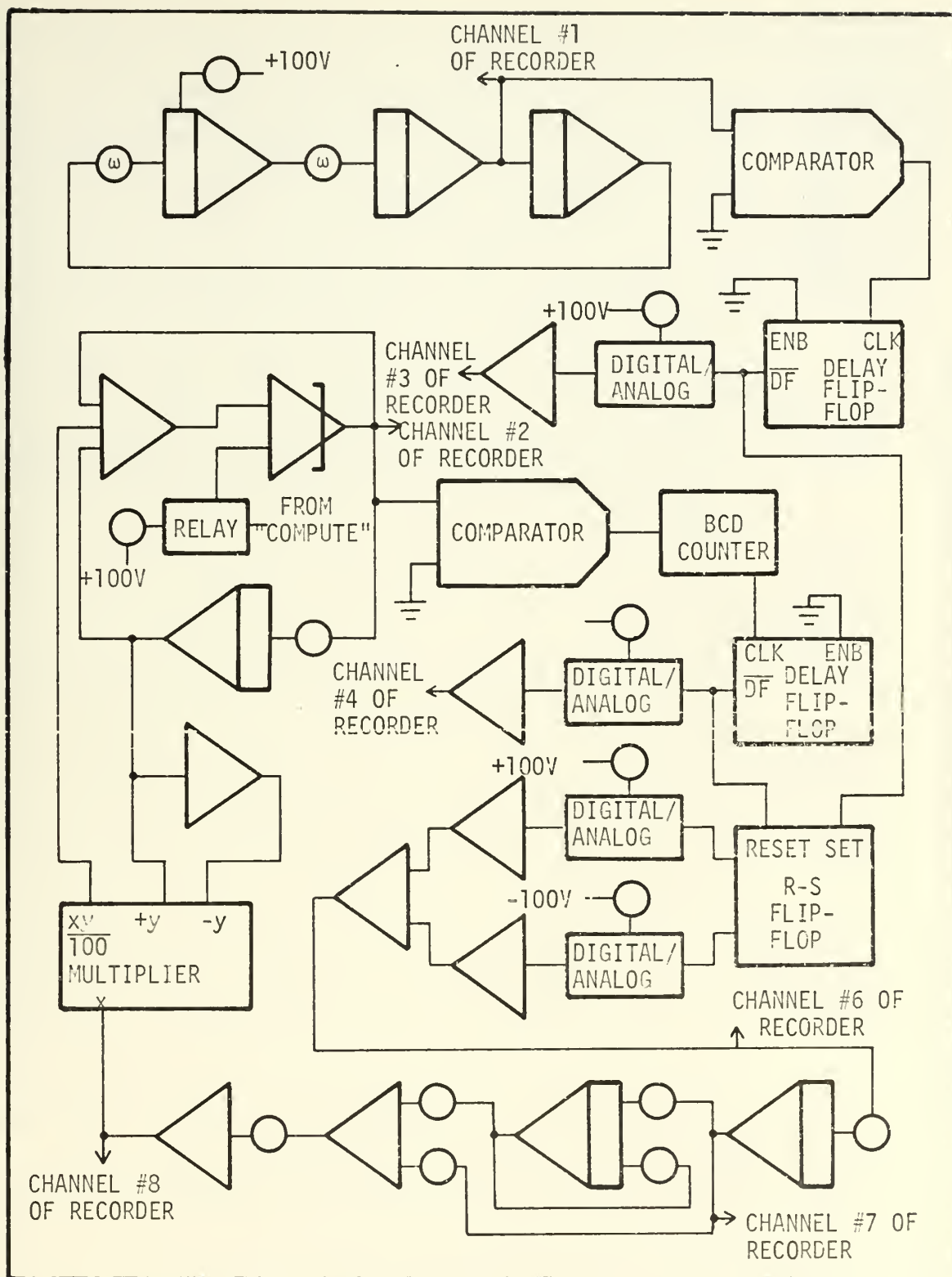


Figure III-B-6. The Complete Analog Simulation Program of the Phase-Locked Loop System.

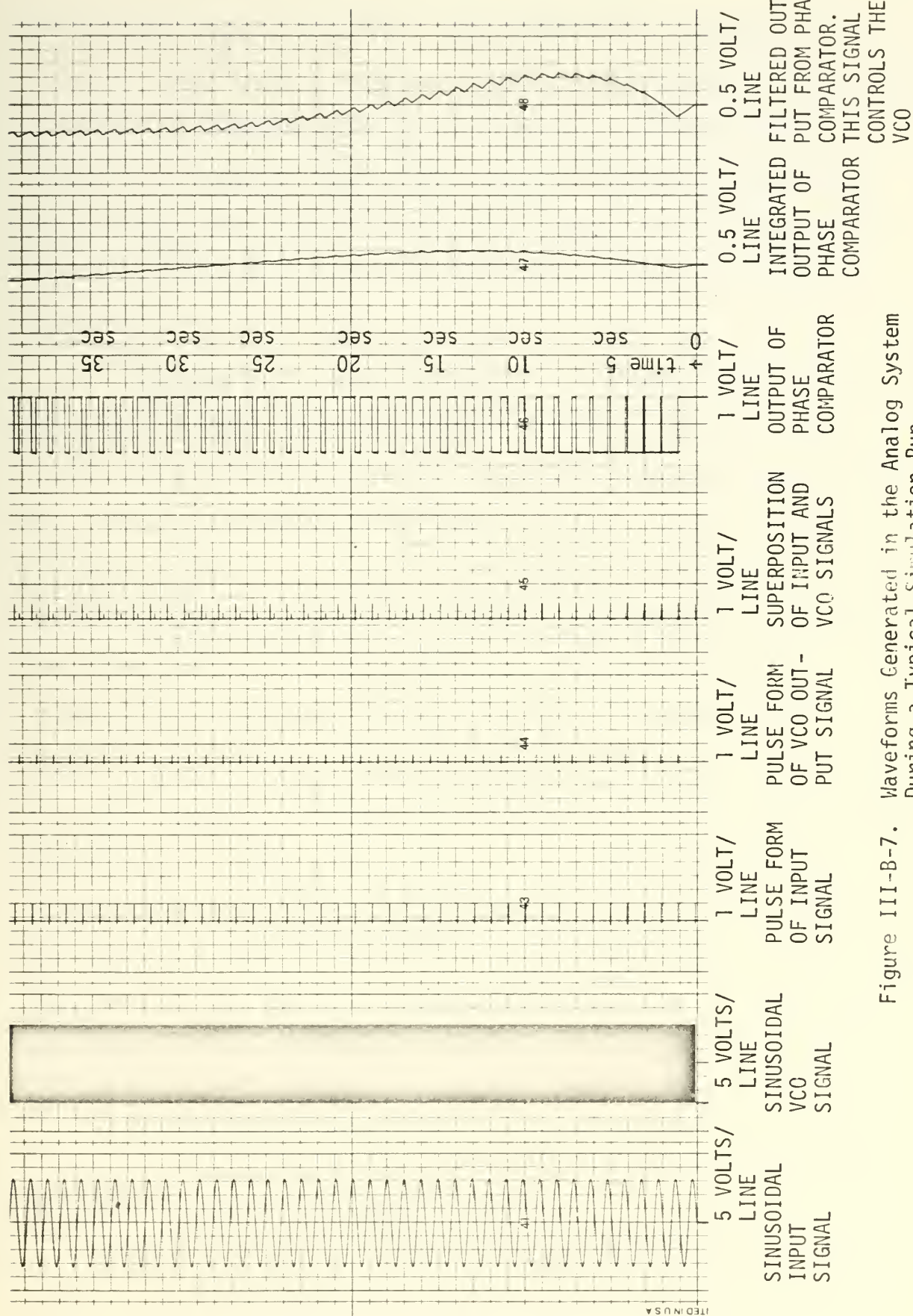


Figure III-B-7. Waveforms Generated in the Analog System During a Typical Simulation Run.

are the only required waveforms. Nevertheless, the sine waves of channels 1 and 2 were recorded to indicate how the pulsed waveforms were generated and demonstrate the action of the VCO countdown circuit. Channel 5 is a superposition of the input and VCO pulses with the VCO pulse of lower amplitude to assist in their identification, and on this channel the phase relationship between the two signals is readily observable.

The process of attaining lock can be followed on Figure III-B-7. The control voltage to the VCO shown on channel 8 is directly proportional to the VCO frequency since only a small frequency difference has been used in this problem and therefore the VCO characteristics may be considered linear. At the start of this particular problem run the VCO control voltage was driven so as to cause the VCO frequency to become lower than its free running frequency for a short time before it recovered and increased in frequency to lock on the input signal. Whether the VCO frequency is forced higher or lower at the beginning of a run is a function of the initial conditions consisting of the frequency and phase of the input signal. It can be seen that after about 30 seconds the average voltage to the VCO remained at a constant value and the frequency of the VCO and the input signal were locked together. Even though the average frequency of the VCO had stabilized, it can be seen that there was still significant instantaneous frequency variations of the VCO over a single cycle of the input signal. This is a characteristic of this particular type of phase comparator and will be discussed much more thoroughly later in this treatise.

Although the VCO average frequency became very close to the frequency of the input signal after about 30 seconds, there was still a significant phase error in relation to the steady state phase

relationship. Due to this phase error the output of the phase comparator was not symmetrical and had an average dc component which was integrated as shown on channel 7 in Figure III-B-7. This increasing voltage applied to the loop filter eventually caused the VCO to shift frequency until the two signals were 180 degrees out of phase, at which time the integrator output was maintained at a constant average value. Thus it can be seen that it took the system longer to integrate out all phase error than it did to attain a relatively close frequency synchronization.

From the Bode plot of Figure III-A-5 it was shown that the loop transfer function has a phase margin of 55 degrees, which would indicate a well damped system. This is verified from Figure III-B-7 where it is seen that the system does not exhibit any overshoot. In addition, the system response shown in Figure III-B-7 appears to be quite slow, and the majority of this thesis shall be devoted to studying ways to improve the system's performance.

C. DIGITAL SIMULATION

The digital simulation phase of the experimental investigation was accomplished on an IBM 360/67 digital computer using both the batch and time sharing modes of processing. Initial simulation attempts were made using both the IBM Continuous System Modeling Program (CSMP) and the IBM Digital Simulation Language (DSL) which are user oriented programs for the digital simulation of continuous system dynamics. However, marginal results were obtained with these programs due primarily to two basic deficiencies. The first difficulty arose because of an inability to actually access the internal operation of the programs and utilize or modify certain parameters as the iteration process proceeded, and the

second difficulty was the fact that the programs used single precision arithmetic, yielding truncation and roundoff errors which resulted in program instability. A program was therefore written using the FORTRAN language and double precision arithmetic to obtain a simulation of the phase-locked loop system shown in Figure III-A-6. The simulation techniques are described below:

1. Input Signal

In the Digital simulation the pulsed input signal waveform was not generated explicitly, but instead a sinusoidal wave was generated by the relationship

$$\text{Input Signal} = \sin (w_{IN}t + \phi) \quad (\text{III-c-1})$$

where w_{IN} is the frequency of the input signal in radians per second and ϕ is the phase of the input signal at zero time. The zero cross over of the sine wave was then used for triggering the phase comparator.

2. VCO

The VCO must be capable of producing a signal whose output frequency can be adjusted by the filtered output voltage of the phase comparator. The VCO output at the i^{th} iteration was computed by the relationship

$$\text{VCO OUTPUT}_i = \sin[\theta_i + 2\pi\Delta T(f_o + K_{VCO} V_i)] \quad (\text{III-c-2})$$

where

$$\theta_i = \sum_{j=0}^{i-1} 2\pi\Delta T(f_o + K_{VCO} V_j) \quad , \quad (\text{III-c-3})$$

ΔT is the time interval between iterations, f_o is the free running VCO frequency, K_{VCO} is the gain of the VCO in cycles/sec-volt, and V_i is the value of the filter output in volts at the i^{th} iteration. Here, as with the input signal, the simulated waveform is a sinusoid and the pulsed form of the signal is not generated explicitly.

3. Phase comparator

The objective of the phase comparator is to generate a waveform which is switched to $+V$ by the occurrence of a pulse of the input signal and switched to $-V$ by a pulse from the VCO. The presence of the input or VCO pulse is determined by using logical statements to detect the zero crossovers of their respective sinusoidal signals. The existence of a pulse is indicated when the product of the function value for the present and the previous iteration is negative and the waveform is going from a negative to a positive value. The input and output of the phase comparator is shown in Figure III-C-1. The voltage levels of the phase comparator output used in the simulation were plus and minus one volt, thus giving the phase comparator a gain of $1/\pi$ volts/radian.

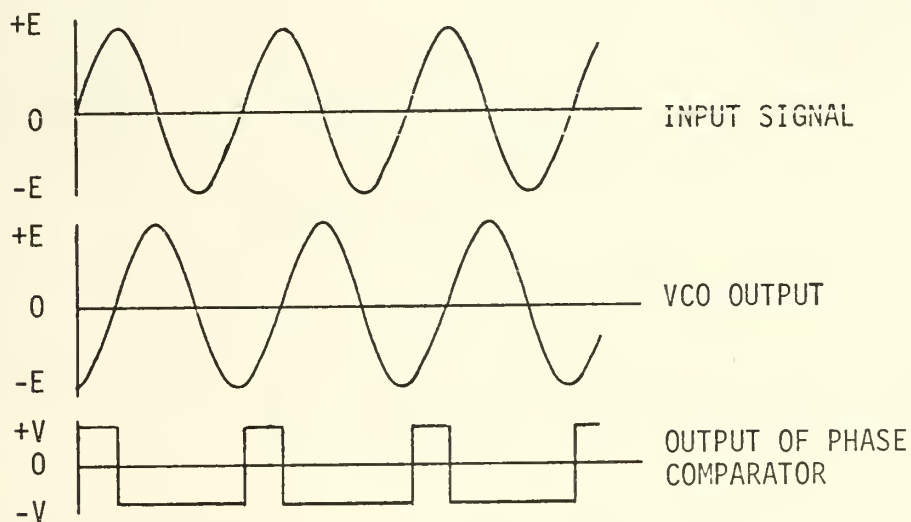


Figure III-C-1. Operation of the Phase Comparator Used in the Digital Simulation.

4. Filter

The first step in the loop filter dynamics is to integrate the output of the phase comparator. Since the waveform from the phase comparator is a constant value voltage with its polarity switched at specified iteration times, there is no need for complicated integration

techniques. The technique used was the basic rectangular integration method using the formula

$$Y_i = Y_{i-1} + \Delta T X_i \quad (\text{III-c-4})$$

where Y_i is the value of the integral and X_i is the input waveform from the phase comparator at the i^{th} iteration.

The lead-lag filter transfer function can be broken up as shown in Equation III-b-2 and then the integral expression solved for z as shown in Equation III-b-5. The relationship between the variables at some arbitrary time is shown in Figure III-C-2. In Figure III-C-2 e_{in} has been plotted as a straight line since it is the integral of a rectangular

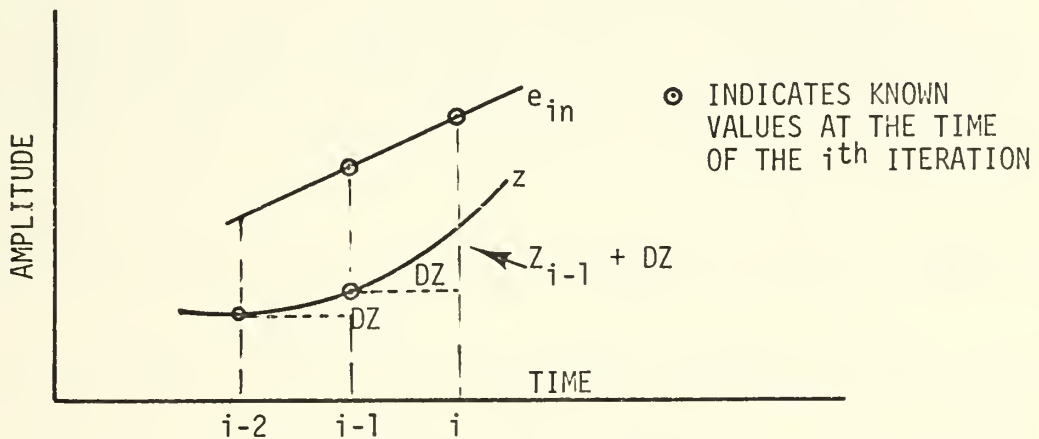


Figure III-C-2. Relationship Between Variables Used in the Lead-Lag Compensator Transfer Function.

waveform and therefore it will be a linear function with changes of slope occurring only at the beginning or end of an integration step interval. The function z has been represented on the sketch by an arbitrary curved line. The points on each curve whose values are known as a result of previous calculations are shown circled in Figure III-C-2, and an estimate of the value of z at the i^{th} iteration can be made by using the fact that z is a continuous function during the iteration interval and making an assumption, based on the problem dynamics, that its value

does not change radically between iterations. The first estimate of z_i , denoted by $z_{i,1}$, can be given by

$$z_{i,1} = z_{i-1} + (z_{i-1} - z_{i-2}) . \quad (\text{III-c-5})$$

Using the first estimate of z_i it was possible to perform the integration of Equation III-b-5 in discrete form and obtain a second estimated value for z_i and then repeat the integration process using the second value to obtain a third or until the system met a specified convergence criterion so that the difference between two successive estimates of z_i was less than a specified amount. It can be seen from the sketch of Figure III-C-2 that now a trapazoidal integration technique must be used instead of the rectangular method used earlier. The equation for the integration process for obtaining $z_{i,k}$, which is the k^{th} estimate of the value of z_i , is given by

$$z_{i,k} = z_{i-1} + \frac{1}{2} b \Delta T [(e_{IN_{i-1}} - z_{i-1}) + (e_{IN_i} - z_{i,k-1})] . \quad (\text{III-c-6})$$

When the prescribed convergence criterion has been met the final value of z_i obtained from Equation III-c-6 is used to solve for e_o by using the second relationship of Equation III-b-3. The equation for e_o expressed in discrete form appears as

$$e_{o_i} = \frac{b}{a} e_{IN} - z_i \left(\frac{b}{a} - 1 \right) . \quad (\text{III-c-7})$$

This value of e_{o_i} is then applied to the VCO as V_i of Equation III-c-2 to obtain the VCO output for the i^{th} iteration.

5. Determination of the Time to Lock

One important measure of the system performance is the time required for the system to attain lock when starting from a given set of initial conditions. The determination of exactly what set of conditions

must be met before the system is said to be in lock is a somewhat arbitrary decision, and two separate criteria will be used in this work. One criterion was based upon frequency relationships and is referred to as frequency lock, and the other criterion was based upon phase relationships and called phase lock.

In the determination of frequency lock it was not possible to use the instantaneous value of the VCO frequency due to its wide variations, and therefore it was first necessary to compute the average value of the VCO output. The average value of the VCO frequency was calculated over one period of the input waveform by summing the VCO output at each computation interval for the last n intervals and then dividing by n , where n was the period of the input signal divided by the computation time interval. A threshold value was then selected and a determination made as to whether the absolute value of the input frequency minus the VCO frequency was less than this threshold. At the first occurrence of the event where the magnitude of the error became less than the threshold, the value of the current problem time was recorded as the time of frequency lock, and this lock time was held for the remainder of the problem or until lock was broken by the error again becoming greater than the threshold. The threshold value could be varied to observe the effects of using different criterion for determining frequency lock.

Phase lock has been defined as the condition where the VCO pulses occur within a specified range of their steady state phase relationship with respect to the input signal. For the circuit being studied the steady state condition is when the phases of the input and the VCO signals differ by 180 degrees, or when the time of the VCO pulse t_{VCO} and the time of the input pulse t_{in} are related by

$$t_{vco} = t_{in} + \frac{1}{2f_{in}} \quad . \quad (III-c-8)$$

When the absolute value of $(t_{vco} - t_{in})$ first becomes less than a specified threshold value then the current value of the problem time is recorded as the value of phase lock, and this time of phase lock will be retained until the end of the simulation or until the magnitude of the error again becomes greater than the threshold.

A complication which arises with the above system, as with any system which utilizes a threshold detection criterion, is that even for very slight changes in system performance it is possible to record rather large jumps in the parameter being measured. This situation can be explained using Figure III-C-3 which shows a typical plot of the system error (either frequency or phase) as a function of time together with the threshold value T_{tv} . For the solid curve the lock time would be recorded as time t_1 , which is the time the error first comes within

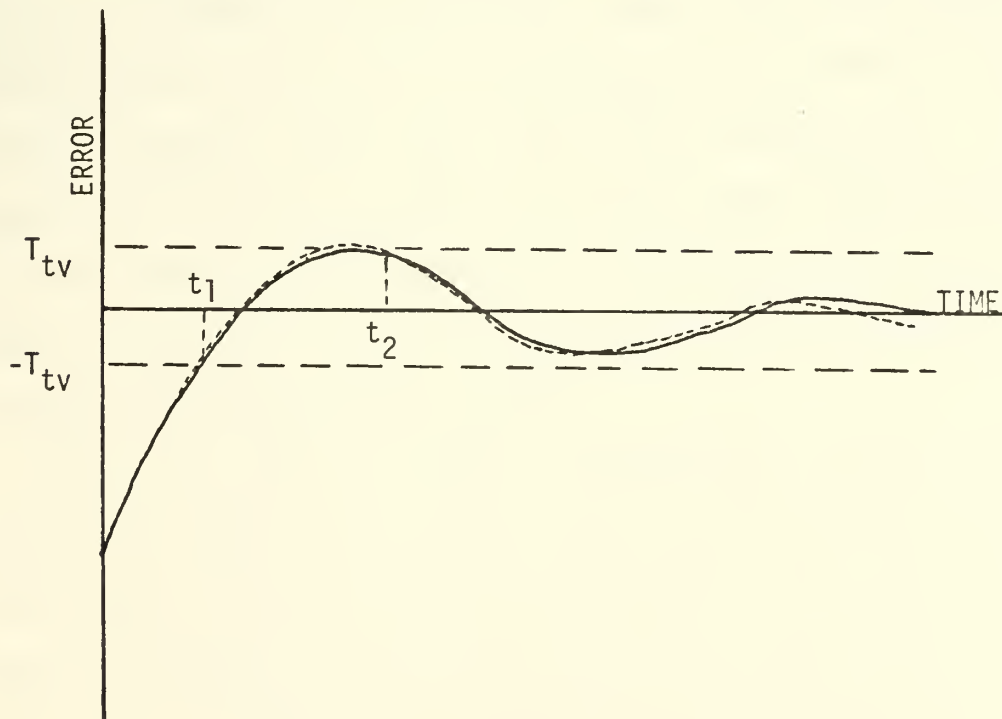


Figure III-C-3. Characteristics of a Threshold Detection Device.

and remains within the threshold limits; while for the dashed curve, which differs only slightly from the solid curve, the time of lock would be recorded as t_2 . Therefore, even though the system operating characteristics differ by only a small amount as indicated by the similarity of the two curves, the recorded lock times experience a large jump which is not indicative of actual system performance. The occurrence of this jump in lock time due to the threshold detector will be observed later in some of the experimental results, and care must be taken to discriminate between the jumps which are due to the threshold detector characteristics, and the jumps which occur in the system due to the inherent operating characteristics of the system.

6. Complete Digital Program

The complete digital 'computer program used to simulate the operation of the phase-locked loop with a normalized VCO frequency of 1.0 cps is included at the end of this thesis. This basic program was later modified to allow iterative computations to be made for various values of frequency, phase, gain, and filter characteristics. The program was also modified to adapt to different types of phase comparators, and these specific modifications will be discussed later in Section V. However, none of these modifications affected the basic simulation procedures presented in this program.

The graphic output of a typical simulation run is shown plotted as a function of time in Figure III-C-4 for the operating conditions consisting of a gain of 0.002, an input frequency of 1.1 cps, and an initial phase of 90 degrees. Part (a) of Figure III-C-4 shows the input pulse train, part (b) gives the VCO pulse train, part (c) shows both the instantaneous frequency error ($f_{in} - f_{vco}$) and the average frequency

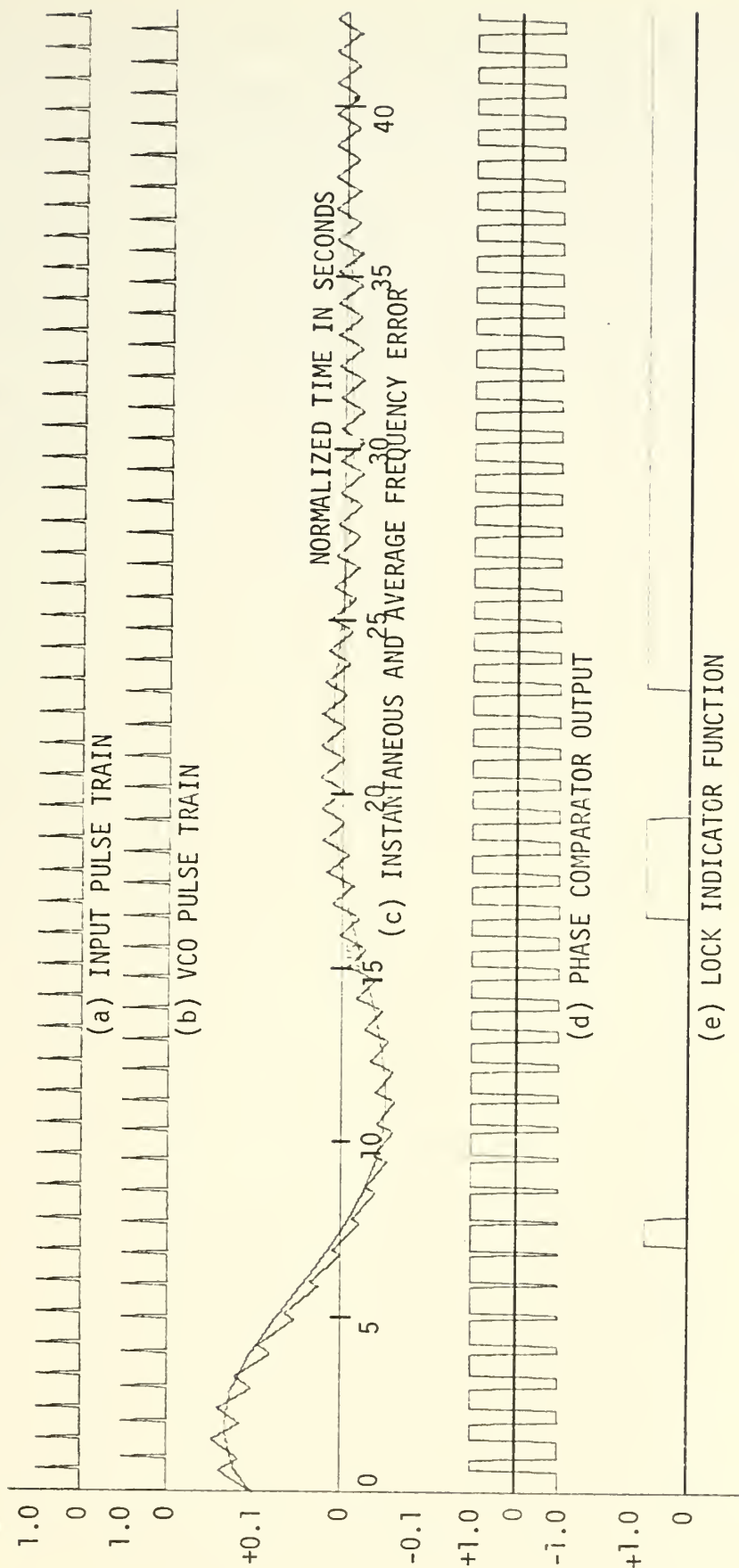


Figure III-C-4. Various System Waveforms Obtained Using the Digital Simulation Program and Plotted as a Function of Time.

error ($f_{in} - f_{avg}$), part (d) shows the output of the phase comparator which is the voltage waveform fed to the loop filter, and part (e) shows a lock indicator function which is +1.0 when the difference between the input and the VCO frequency is less than one percent and zero otherwise. Many other forms of output will be presented later, such as plots of frequency-lock and phase-lock times as a function of frequency or phase, but these plots will be discussed at the time they are presented.

IV. RESULTS OF EXPERIMENTAL INVESTIGATION

The system simulation techniques were described in Section III together with a graphical portrayal of the simulation results for a specific set of system parameters and initial conditions. In this section a detailed analysis will be given of the system performance as a function of each of the system variables and of the initial conditions.

Because of the quasi-sample data characteristics and the nonlinearity of the system under study, all previous investigations have been based on various approximations; and although some of the analyses have yielded exact results for the approximate systems under study, no one has yet been able to achieve an exact mathematical solution to the actual system. Nor is it considered obvious that an analytical solution actually exists. Nevertheless, the research performed here utilized an exact simulation of the entire system, and since the output is not expressible in closed form, it is necessary that most of the experimental findings be presented in graphical format. Due to the normalization of all parameters and inputs as explained in Section III, the curves may be readily interpreted and applied to any set of operating conditions. These normalized results give a very good insight and understanding into all aspects of the system's performance and provide a firm basis for system design.

An effort has been made to test the effects of each variable independently by holding all other variables fixed and manipulating only that parameter under consideration. However, due to the detailed interaction between system parameters, it has been necessary in almost every case to give the results as a family of curves with each curve representing a different set of operating conditions. In this way a better overall

representation may be made of the system operation as a function of the specific variable under study and its interactions with the other system parameters.

A. LOCK PERFORMANCE AS A FUNCTION OF INITIAL PHASE DIFFERENCE

The time required for the VCO to lock onto the input signal is a function of the initial phase relationship between the input signal and the VCO. For the sawtooth phase comparator characteristics used in this simulation and shown in Figure III-A-3, the average output voltage over a complete cycle will be positive if the phase error is greater than 180 degrees and negative if the phase error is less than 180 degrees.

The effect that the initial phase relationship has on the time required for the system to lock is shown in Figure IV-A-1. The input signal is represented as starting at time zero and may be represented by

$$S_{in} = f[(\omega_0 + \Delta\omega)t] \quad (IV-a-1)$$

where ω_0 is the free running frequency of the VCO, and the VCO signal may be represented by

$$S_{vco} = f[\omega_0 t - \phi_0] \quad (IV-a-2)$$

where ϕ_0 is the phase angle by which the VCO lags the input signal.

The determination of which phase relationships aid and which hinder the locking operation of the loop is easily made by noting that if the input frequency is higher than the VCO then a positive voltage must be applied to the VCO to adjust its frequency in the right direction, and this in turn requires that the VCO lag the input signal by 180 degrees $\leq \phi_0 \leq 360$ degrees. The above argument is simply reversed for an input frequency that is lower than the VCO frequency.

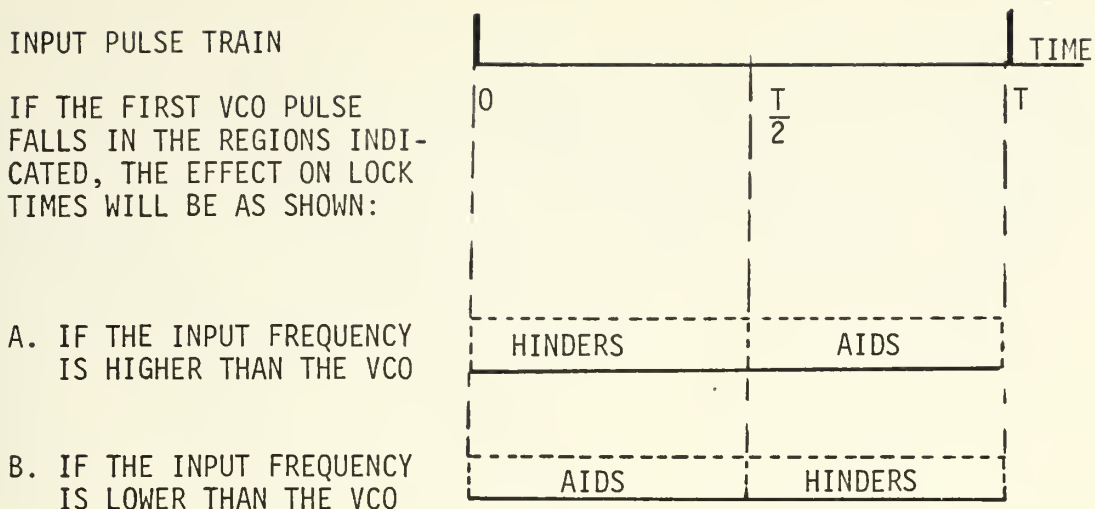


Figure IV-A-1. Effect on Lock Time Caused by the Phase Relationship of the Initial VCO Pulse with Respect to the Input Pulse Train.

The filtered output of the phase comparator is shown in Figure IV-A-2 and IV-A-3 for the condition of high and low input frequency respectively. The curves are plotted for various values of the phase lag angle of the VCO ϕ_0 , where the values of ϕ_0 used are all integral multiples of 27.69 degrees which is one interval of the VCO countdown circuit used in the analog simulation. These figures show the actual corrective voltages which would be applied to the VCO; however, in making these graphs the system was made free-running by opening the feedback circuit to the VCO and thereby allowing the output of the phase comparator to be observed without the complications of feedback.

For an input frequency which is 10 percent higher than the VCO frequency, it can be seen from Figure IV-A-2 that the greatest positive value of the output voltage which is developed at the end of the first cycle occurs when the VCO lags the input by a large amount, and lower values of output voltage result as the phase lag decreases until at $\phi_0 = 180$ degrees the output voltage at the end of the first cycle is zero.

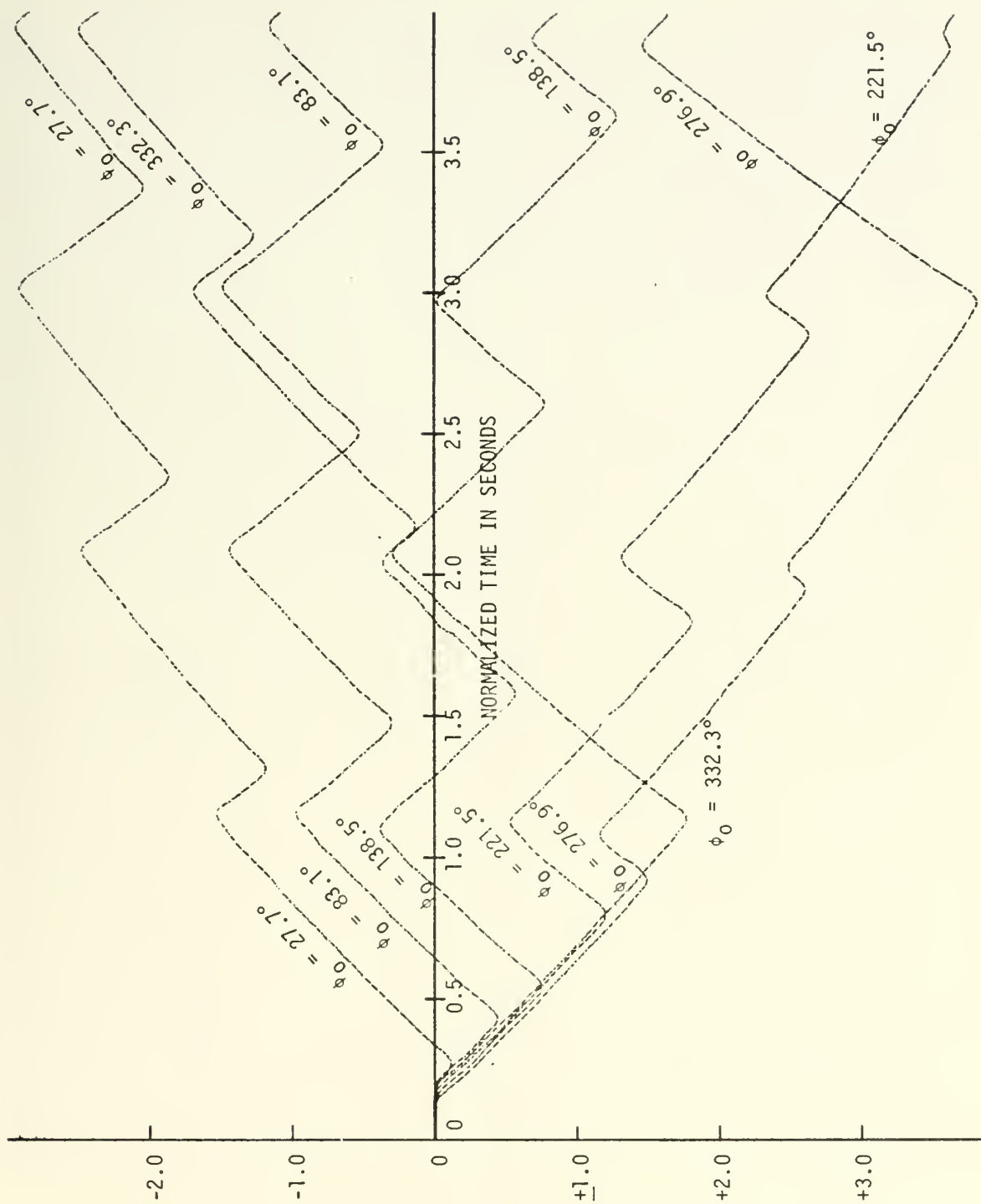


Figure IV-A-2. Filtered Output Voltage of the Phase Comparator for a Normalized Input Frequency of 1.1 cps and for Various Values of the Angle ϕ_0 by Which the VCO Lags the Input Signal.

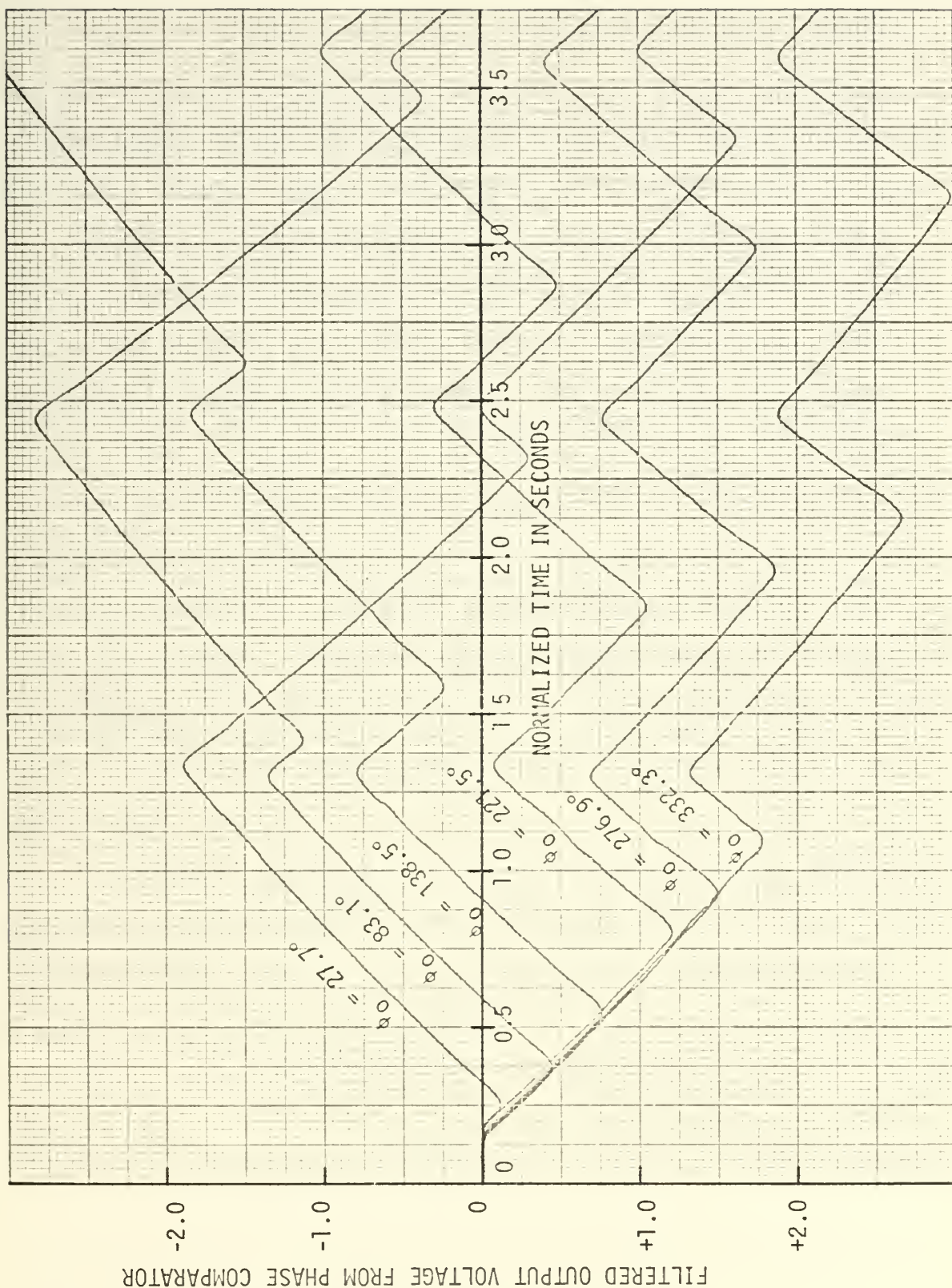


Figure IV-A-3. Filtered Output Voltage of the Phase Comparator for a normalized Input Frequency of 0.9 cps and for Various Values of the Angle ϕ_0 by Which the VCO Lags the Input Signal.

Thus for values of $180 \text{ degrees} \leq \phi_0 \leq 360 \text{ degrees}$ the phase comparator output at the end of the first cycle tends to drive the VCO towards a locking condition, but for a phase lag of less than 180 degrees the voltage output becomes negative and tends to drive the VCO away from lock.

The simple relationship between initial phase and filter output voltage discussed above rapidly becomes more complex as time progresses due to the frequency difference of the two signals which causes the VCO phase lag to become greater each cycle. When the phase difference becomes $(360 + \alpha)$ degrees, the operation is the same as for a lag of α degrees, and the system performance characteristic experiences an abrupt change due to the skipping of a cycle. This cycle skipping phenomenon is shown in Figure IV-A-2 and occurs at the end of one cycle for a phase of 332.2 degrees and at the end of three cycles for a phase of 276.9 degrees. Cycle skipping also occurs in Figure IV-A-3, but there the input frequency is lower and the cycle skipping occurs first for low values of initial phase lag.

An expression giving the time at which the first cycle skipping occurs as a function of the input and VCO frequencies and the angle ϕ_0 by which the VCO lags the input signal will be derived for the free running condition. When the input signal is of a higher frequency than the VCO, the time interval between the first VCO pulse and the second input pulse is given by

$$t_{\text{dif}} = \frac{1}{f_{\text{in}}} - \frac{\phi_0}{360 \times f_{\text{vco}}} \quad (\text{IV-a-3})$$

The amount by which the interval t_{dif} is decreased during each cycle of the input signal is given by

$$\Delta t = \left| \frac{1}{f_{\text{vco}}} - \frac{1}{f_{\text{in}}} \right| \quad (\text{IV-a-4})$$

and a cycle is skipped for the first integer value of N_h where

$$N_h \Delta t \geq t_{dif} \quad . \quad (IV-a-5)$$

Combining the above equations it is possible to solve for N_h as

$$N_h = I \left[\frac{f_{vco} - \phi_o \frac{f_{in}}{360}}{|f_{in} - f_{vco}|} \right] \quad (IV-a-6)$$

where $I[\]$ denotes the greatest integer function which assigns to N_h the largest integer value less than or equal to the expression in brackets. A similar procedure may be carried out for the condition when the input frequency is lower than the VCO, and an expression for N_l may be derived as

$$N_l = I \left[\frac{\phi_o f_{in}}{360 \times |f_{in} - f_{vco}|} \right] \quad . \quad (IV-a-7)$$

The time of the first skipped cycle may then be given as

$$t = \frac{N + 1}{f_{in}} \quad (IV-a-8)$$

where N may be either N_h or N_l . In the free running situation the system would continue to skip cycles with a frequency ω_{cs} given by

$$\omega_{cs} = |\omega_{in} - \omega_{vco}| \quad . \quad (IV-a-9)$$

Cycle-skipping introduces one of the primary nonlinearities into the system, causing an abrupt change in the output of the phase comparator and reversing the polarity towards which the filter output is tending. If the curves of Figures IV-A-2 and IV-A-3 had been made with the feed-back loop connected, the system would not have demonstrated the predictable cycle-skipping as a function of time, frequency, and phase difference as shown in Equations IV-a-8 and IV-a-9. Also, the relationships shown

in Figure IV-A-1 no longer apply directly when cycle-skipping takes place. For example, for the input frequency higher than the VCO and ϕ_0 near 360 degrees, there may not be time to integrate out the phase difference and adjust the VCO before a cycle is skipped, while for a ϕ_0 nearer to 180 degrees there will not be as large a corrective voltage developed, but it will have a longer period of time to integrate over, and as a result the VCO may be able to adjust sufficiently to prevent a cycle from being skipped. The exact performance at any time is always a complex interaction of all the system characteristics.

Using the digital simulation program, the time at which the average VCO frequency reached and remained within 1.0 percent of the input frequency was computed for each 5 degrees by which the VCO signal initially lagged the input signal. The results for three different values of input frequency are shown plotted in Figure IV-A-4. The lock times shown in Figure IV-A-4 correspond to the theory put forth in Figure IV-A-1, and for values of ϕ_0 between 0 degrees and 180 degrees the time to lock for an input frequency higher than the VCO averages greater than that for an input frequency lower than the VCO, which is as expected. The lock time for the condition where the input frequency equals the VCO frequency is in general less than the lock time when there is a frequency offset, and the time required to lock exhibits an approximately symmetric curve about the steady state phase angle which is 180 degrees.

Figure IV-A-4 shows some sharp jumps in lock times, which at first might appear to be due to irregularities in the simulation technique. However, a detailed study of the phenomenon using the analog simulation has shown that this is a characteristic of the nonlinearity of the system, and that a smooth increase or decrease in lock time as a function of phase is not to be expected. The analog output showing the effect of

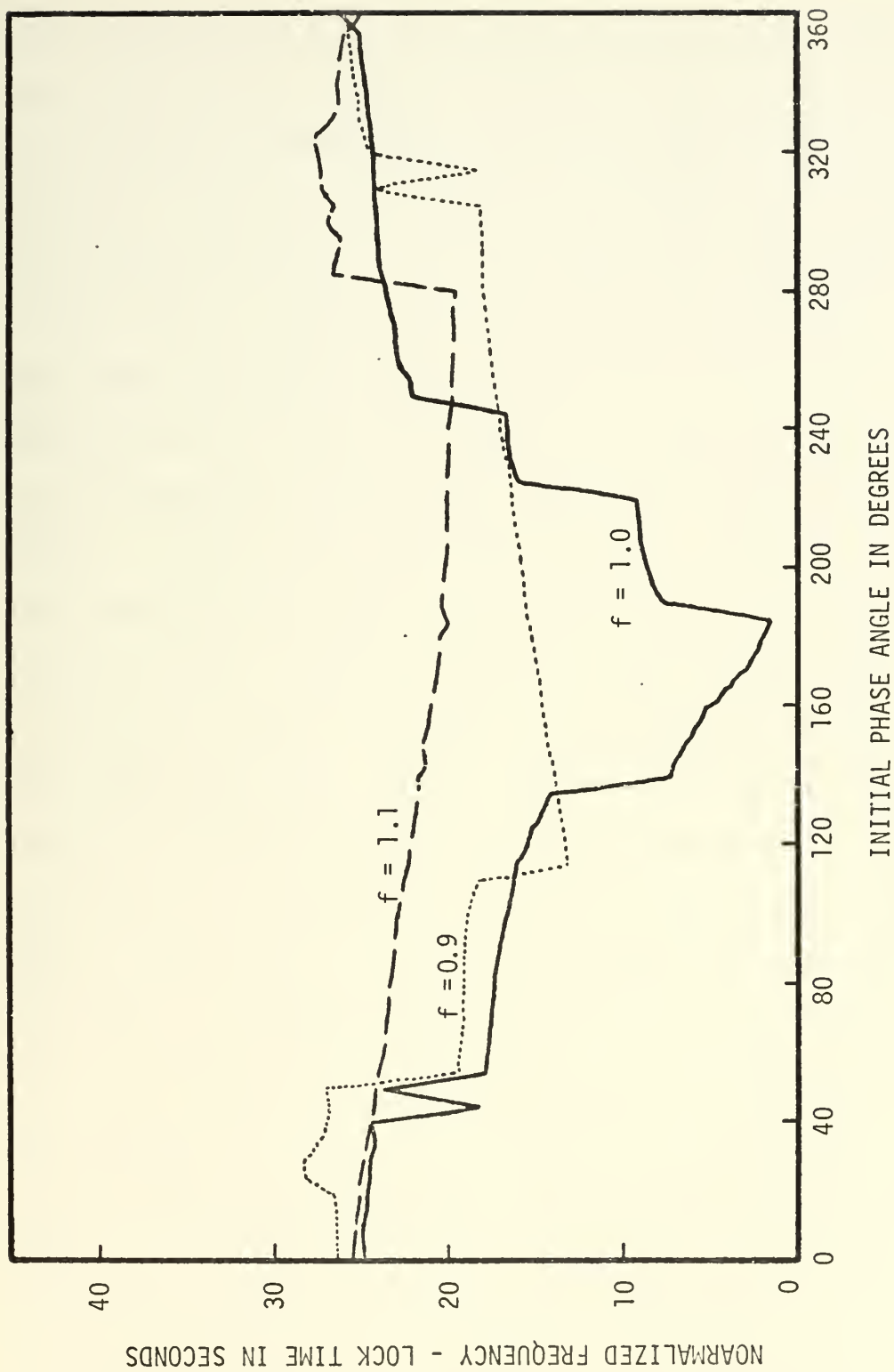


Figure IV-A-4. Normalized Time to Attain Frequency Lock as a Function of the Initial Phase Angle for Several Values of the Normalized Input Frequency.

phase variations on lock time is given in Figure IV-A-5. For initial phase differences ϕ_0 between 138.5 degrees and 221.5 degrees there is no cycle skipping and the system behaves in accordance with linear theory as shown in Figure IV-A-1 in that the greater the value of ϕ the quicker the system attains lock. It is also noted that in this region the plot of lock time as a function of phase would be expected to give a smooth continuous curve without sharp discontinuities. This corresponds with the data shown in Figure IV-A-4 where the curves for both higher and lower frequencies are continuous in the central region about $\phi_0 = 180$ degrees. As the initial phase lag increases, a point is reached where the system skips one cycle as shown by the curve for $\phi_0 = 249.2$ degrees on Figure IV-A-5. This cycle-skipping causes a sudden, sharp increase in the time to lock which appears as a discontinuity on the curve of lock time versus phase. As ϕ_0 is further increased beyond this point, the time of the first cycle-skipping decreases and the lock time gradually and smoothly decreases until the point $\phi_0 = 332.3$ degrees, when another sharp increase occurs in the lock time because the system now has skipped two cycles. A similar sequence of events occurs as ϕ_0 is decreased, with the overall result that when the lock time is plotted as a function of phase as done in Figure IV-A-4 there must be discontinuities in the curve at every instance where a change is made in the number of skipped cycles. Between the regions where transitions take place in the number of skipped cycles the lock time is a smooth continuous function of initial phase.

B. LOCK PERFORMANCE AS A FUNCTION OF INITIAL FREQUENCY DIFFERENCE

In order to assist in the study of system performance as a function of the initial frequency difference, the digital computer was used to calculate the time of attaining frequency lock for each incremental

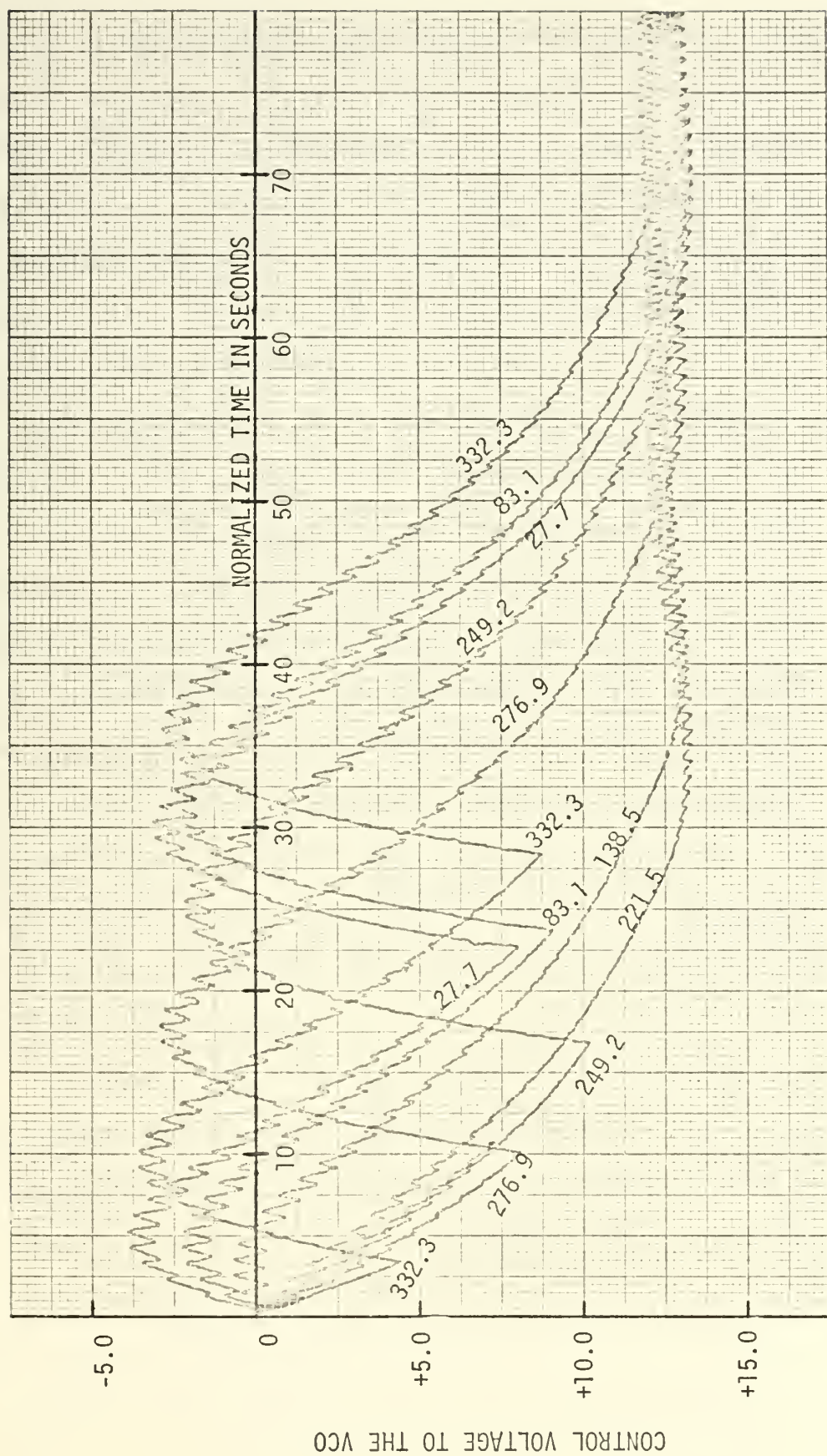


Figure IV-A-5. Analog Simulation Results Showing the Voltage to the VCO as a Function of Time for an Input Frequency of 1.05 cps and for Various Values of the Initial Phase Angle.

change in the normalized input frequency of 0.005 cps. The resultant family of curves is shown in Figure IV-B-1 for three values of the phase angle ϕ_0 by which the VCO lagged the input signal. These curves show deviations of ± 15 percent in the normalized frequency offset, and demonstrate the complex relationships between frequency and phase, whereby only a slight change in input frequency may reverse the relationship between phase and lock time.

From Figure IV-B-1 it is seen that for $\phi_0 = 180$ degrees, which is the steady state phase relationship, there is a sharp dip in the time required to lock for input frequencies near the VCO frequency. However, the reduced lock times are not symmetrical about the VCO frequency. This is due to the simulation technique used, where the VCO signal started at time zero and the input signal started at a later time which was specified by the angle ϕ_0 . Since the VCO signal came first, the output of the phase comparator was always negative at time zero, and this negative output served to assist the lower frequencies to lock sooner. The situation was simply reversed when the simulation was run with the input signal occurring first, thus demonstrating that the initial conditions affect the output in many ways.

A second family of curves is shown in Figure IV-B-2 and was also made using the digital simulation, but employing a different criterion for determining when the system attained lock. Here the time to lock was defined as the time when the phase of the input and VCO signals first reached and remained within 10 percent of their steady state value, and this type of system lock was called 'phase lock' in contrast to the 'frequency lock' shown in Figure IV-B-1. The threshold value of 10 percent is an arbitrary figure and is not critical to the discussion presented here. Changes in the threshold level used in determining phase

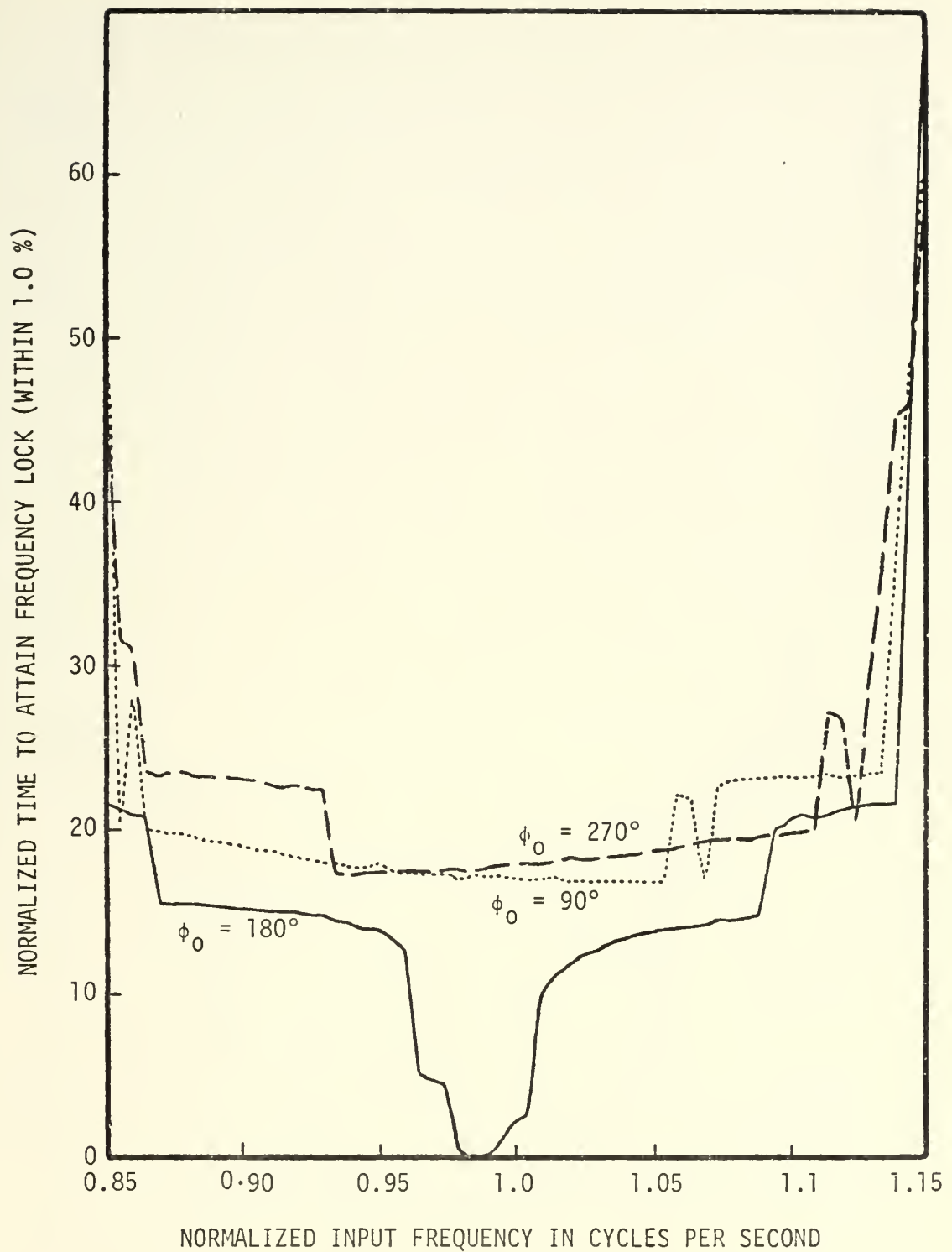


Figure IV-B-1. Normalized Time Required for the System to Attain Frequency Lock as a Function of the Input Frequency for Several Values of the Initial Phase Angle.

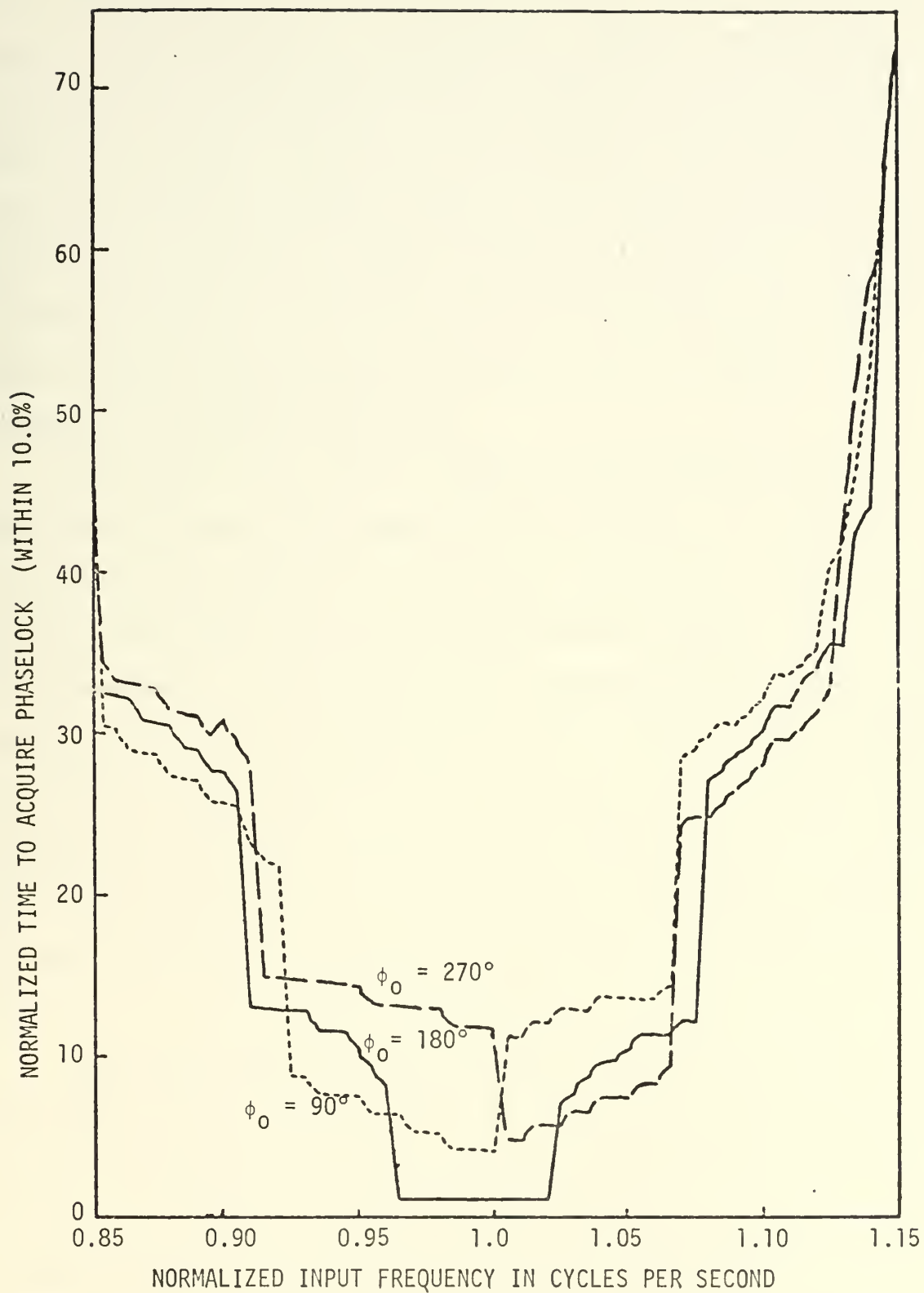


Figure IV-B-2. Normalized Time Required for the System to Attain Phase Lock as a Function of the Input Frequency for Several Values of the Initial Phase Angle.

lock merely shifts the curve up or down along the normalized time scale and also shifts the points of discontinuity slightly along the normalized frequency axis, but the overall pattern of the curves remains the same. The curves of Figure IV-B-2 show a slight deviation from being symmetrical about the VCO frequency, with the lower frequencies having a slight advantage in attaining lock due to the VCO pulse occurring first in time as explained above. However, except for the slight favor shown to the lower frequencies, the curves exhibit a very uniform behavior with respect to both frequency and phase.

A comparison of the curves of phase lock and frequency lock as a function of frequency show some predominant characteristics. First, the effect of initial phase on the lock time is much more pronounced for the curves showing phase lock than for those showing frequency lock. Second, close frequency synchronization within a specified length of time can be obtained with a phase-locked loop over a wider range of input frequency than can close phase synchronization. In effect, it takes much longer to integrate out the phase differences than it does to force the VCO to within a specified tolerance of the input phase. This effect was demonstrated more clearly in Figure III-B-7 and discussed in Subsection III, B,5.

It has been shown previously in Figure IV-A-5 that for a fixed value of input frequency, a slight change in input phase can cause sharp discontinuities in the lock time. A similar effect is noted in Figures IV-B-1 and IV-B-2 where, for a constant phase, a slight change in frequency sometimes causes a large change in lock time. This effect was studied using the analog computer, and a continuous plot of the filtered output voltage from the phase comparator which controls the VCO is shown plotted in Figure IV-B-3 for two values of the initial phase ϕ_0 .

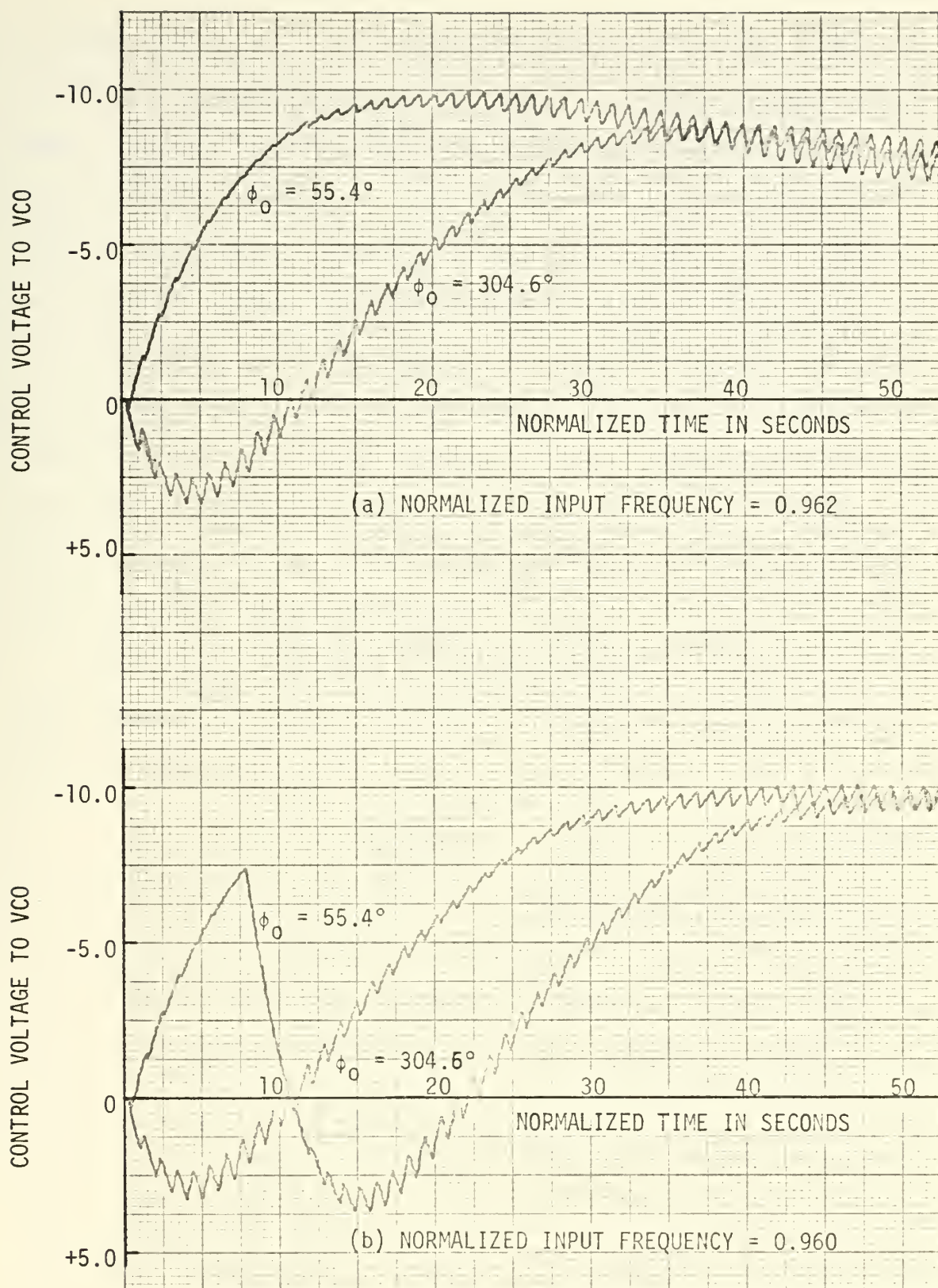


Figure IV-B-3. Demonstration of How the System Performance Changes About a Critical Frequency.

In Figure IV-B-3 part (a) the normalized input frequency was 0.962 cps, and the system acquired lock without any cycle skipping for both phases shown. However, in Figure IV-B-3 part (b) the input frequency was reduced by only 0.002 cps to 0.960 cps, and the system exhibited marked changes in performance. Now the system response for $\phi_0 = 55.4$ degrees was nonlinear, and one cycle was skipped resulting in an increase in the lock time. This figure demonstrates the abrupt changes that take place in system behavior at the point where cycle skipping occurs, and similar behavior takes place for any operating condition where there is a change in the number of skipped cycles, thus accounting for the discontinuities which have been observed in the curves of frequency-lock and phase-lock time as a function of input frequency.

Another way of presenting the system performance as a function of the input frequency is shown in Figure IV-B-4 where the average normalized frequency error, defined by

$$f_e = f_{in} - f_{vco} , \quad (IV-b-1)$$

is shown plotted versus the normalized time for various values of the input frequency and with ϕ_0 held at 90 degrees for all curves. Under these conditions the phase-locked loop performs in a linear fashion for input frequencies which differ less than ± 15 percent from the VCO frequency, and within this range the lock time varies as a uniform function of input frequency. However, once the input frequency becomes greater than a threshold value f_s , called the seize frequency, then cycle skipping occurs and the time to lock greatly increases. This condition is demonstrated by the curves for $f_{in} = 1.15$ and $f_{in} = 0.85$ where in each case three cycles are skipped before attaining lock. As the initial frequency offset becomes even greater, the number of skipped cycles

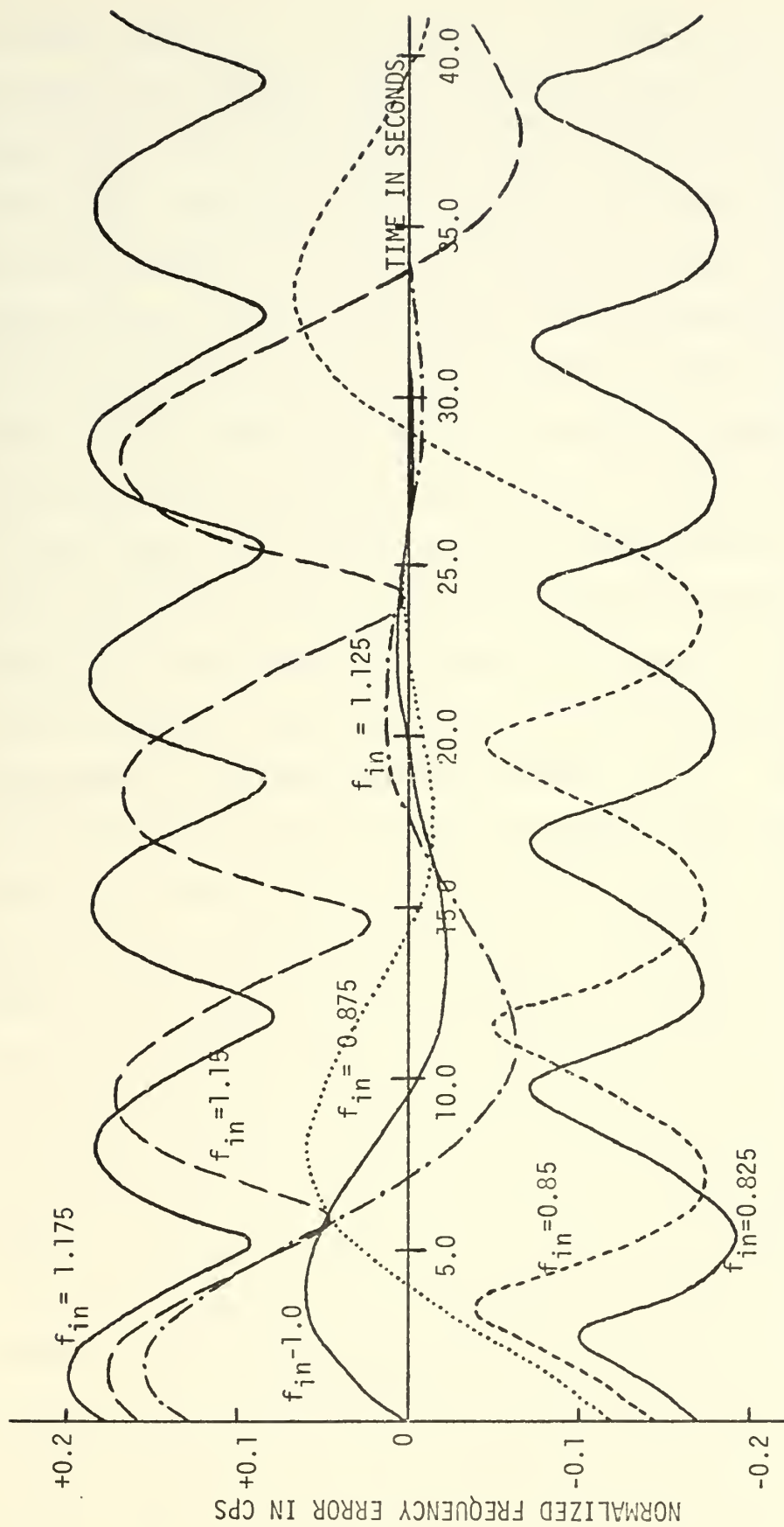


Figure IV-B-4. Plot of Normalized Frequency Error ($f_{in} - f_{vco}$) Versus Time for Various Values of Input Frequency with $\phi_0 = 90$ Degrees.

increases, and for $f_{in} = 1.175$ and $f_{in} = 0.825$ the system is still skipping cycles throughout the 45 second observation time shown in Figure IV-B-4. The basic phenomenon shown in Figures IV-B-3 and IV-B-4 is the same. However, the curves of Figure IV-B-3 were obtained using the analog computer and shows the instantaneous value of the VCO control voltage, which is directly proportional to the instantaneous frequency of the VCO, and therefore the variations during each cycle are shown. The curves of Figure IV-B-4 were made with the digital computer and here the instantaneous VCO frequency was averaged over the period of one cycle of the input signal. This averaging process explains why the curve is smooth and does not show the sawtooth like variations which occur during each cycle. The averaging also accounts for the cusp, which occurs when a cycle is skipped, being rounded off in the digital output while it is a sharp peak in the analog simulation output.

Up to this point the range of input frequency under study has been restricted to about ± 15 percent of the VCO frequency, and although the system behavior varies within this range, it still remains within relatively narrow bounds. As the frequency difference between the input and the VCO increases beyond ± 15 percent the system performance changes, and longer times are required for the system to attain lock. Figure IV-B-5 was obtained using data from the digital simulation with $\phi_0 = 180$ degrees, and shows how the time of frequency lock increases with increasing frequency deviation for input frequencies larger than the VCO frequency. Similar data is shown in Figure IV-B-6 and was obtained using the continuous analog simulation and an increased value of gain which was four times the gain used in all previous simulations. Here, due to the increased gain, the region of the curve having a relatively flat response was extended to about ± 20 percent frequency deviation, and beyond this

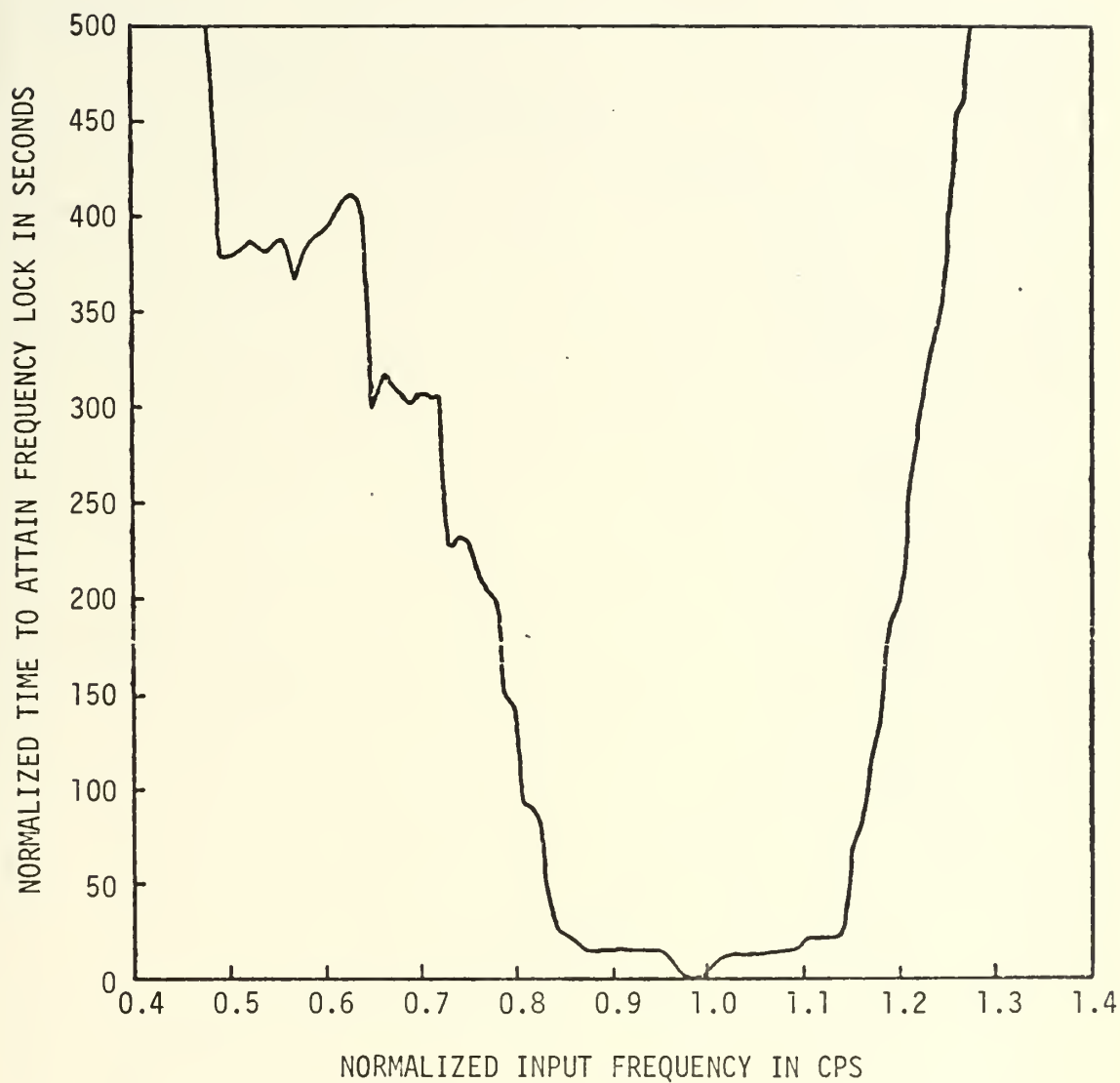


Figure IV-B-5. Digital Simulation Data Showing Time Required to Attain Frequency Lock as a Function of Input Frequency for Large Values of Frequency Offset and for an Initial Phase of 180 Degrees.

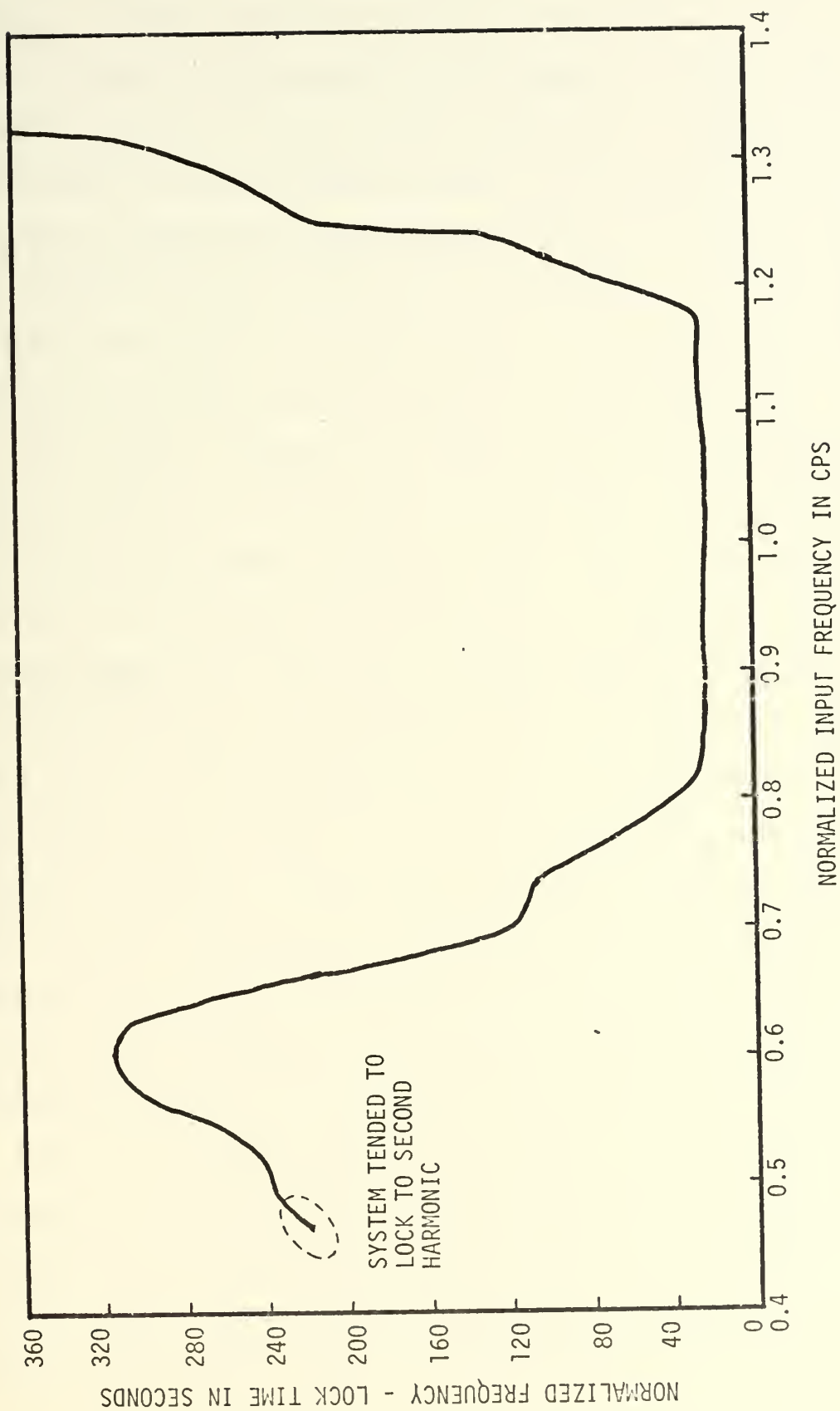


Figure IV-B-6. Analog Simulation Data Showing the Time Required to Attain Frequency Lock for Large Values of Frequency Offset with an Initial Phase of 180 Degrees.

region the time to lock increased rapidly with increasing frequency offset. For input frequencies which were higher than the VCO, the system continued to lock regardless of the amount of frequency offset; however, the time to lock soon became exorbitant. Several test runs were made using large frequency offsets, and normalized lock times in excess of 2,000 seconds were obtained. Although such long lock times are prohibitive for most applications, there might be some uses where synchronization time is not a prime factor, and the important characteristic being that the system does always attain lock.

The fact that a second order system using a sine comparator and a perfect integrator in the filter can always attain lock when operating in a noise-free environment was proven by A.J. Viterbi [Ref. 12]. This proof was later extended by B.J. Leon and L.L. Cleland [Ref. 33] to cover a second order system with a perfect integrator in the filter and employing any type of phase comparator whose characteristics were odd with respect to the zero phase error axis. However, these unlimited lock ranges did not result if the filter characteristics did not include a perfect integrator. The particular system under study in this research does include a pure integrator in the loop filter characteristics, and theoretically unlimited lock ranges could be expected in theory. In the analog simulation the actual lock range was limited by the amplifier saturation voltages and by the dynamic characteristics of the VCO.

At the low frequency end of the curve shown in Figure IV-B-6 the lock time began to decrease. However, as the normalized input frequency approached 0.5 cps the system tended to lock to the second harmonic of the input signal, and when this occurred the lock time decreased to the order of 15-20 seconds. Whether the system would lock to the fundamental

or a harmonic was a function of not only the input frequency, but also of the input phase and the system gain.

In summary, it has been demonstrated that the initial frequency offset is one of the prime factors affecting the system performance, and, while there is a region about the VCO frequency where the loop is relatively insensitive to frequency changes, once the frequency deviation becomes greater than a threshold value the lock time increases rapidly. The only limitations found on the maximum frequency offset which would attain lock were due to simulation equipment saturation and computer run time limitations. However, for low values of input frequency, the system tended to lock on harmonics.

C. LOCK PERFORMANCE AS A FUNCTION OF GAIN

In the phase-locked loop as in other feedback systems, the loop gain is an important factor in determining the system performance. For second-order systems the effect of gain variations can be described using the damping factor ζ and the natural frequency ω_n . However, for a third-order system these factors are not clearly defined, and therefore the phase margin ϕ_m and closed loop bandwidth BW_{CL} have been chosen as indices of system performance. If the pole and zero configuration of the system filter is maintained as shown in Equation III-b-2 and only the gain is varied, then the phase margin and closed loop bandwidth can be plotted as a function of gain as shown in Figure IV-C-1. The design operating gain of 0.002 is that value of normalized gain which gives the maximum phase margin for the specified pole-zero configuration, and the phase margin decreases quite rapidly as the gain varies in either direction from this design value. The closed loop bandwidth is seen to be an increasing function of gain, but it also exhibits nearly rotational symmetry about the design gain value.

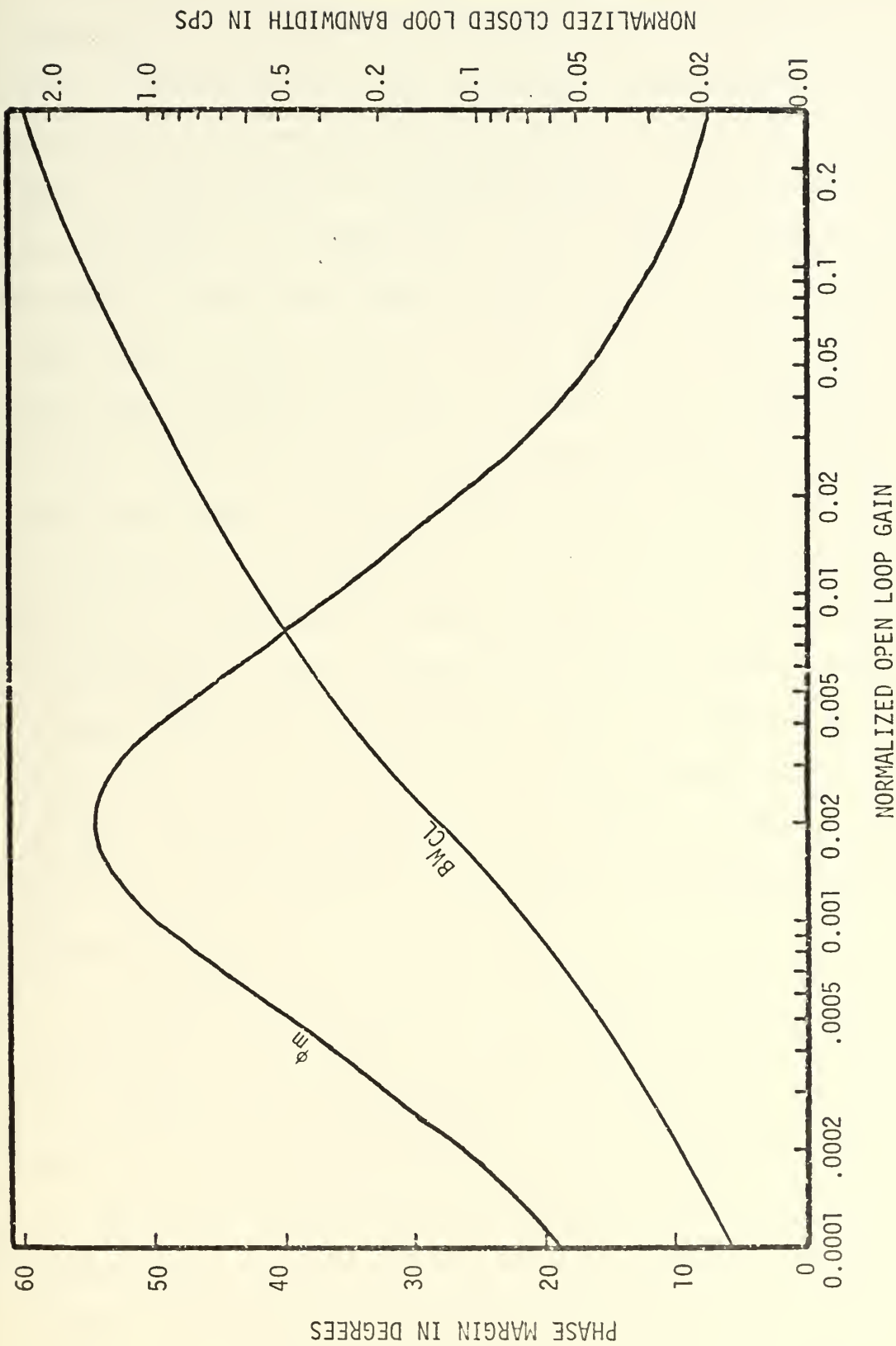


Figure IV-C-1. Phase Margin and Closed Loop Bandwidth as a Function of Gain with the Compensator Zero and Pole Held Fixed at 0.025 and 0.25 Respectively.

Using the digital computer, families of curves were produced to study the variation of the average normalized frequency error as a function of time for various values of loop gain while holding the initial conditions on frequency and phase constant. One such set of curves is shown in Figure IV-C-2 for an input frequency of 1.15 cps and an initial starting phase of $\phi_0 = 180$ degrees. For low values of gain the time required to attain lock becomes very great because there is insufficient amplification to force the VCO to adjust quickly. For very high gain the phase margin decreases, therefore the system tends to become oscillatory and again the time to lock increases slightly because now the VCO oscillates above and below the input frequency, damping out slowly. It is the region of intermediate gain which is of most interest, and in this region the effect of gain is dependent upon both the initial phase and input frequency. This is demonstrated in Figure IV-C-2 where an increase of gain from 0.002 to 0.004 caused a significant reduction in the lock time, while in a similar family of curves made with a smaller initial frequency difference such that no cycle skipping occurred at a gain of 0.002, the same increase in gain made only minor improvements in the lock performance.

The interaction between gain and frequency is displayed in Figure IV-C-3 where the time to achieve frequency lock within one percent is plotted as a function of the input frequency for four different values of normalized gain and for an initial phase of $\phi_0 = 180$ degrees. If the curves for gains of 0.001 and 0.002 are considered first, it is seen that for greater than ± 3 percent deviation in input frequency, the system performs as one might expect, with the higher gain resulting in a shorter time to lock. However, for frequency deviations of less than 3 percent

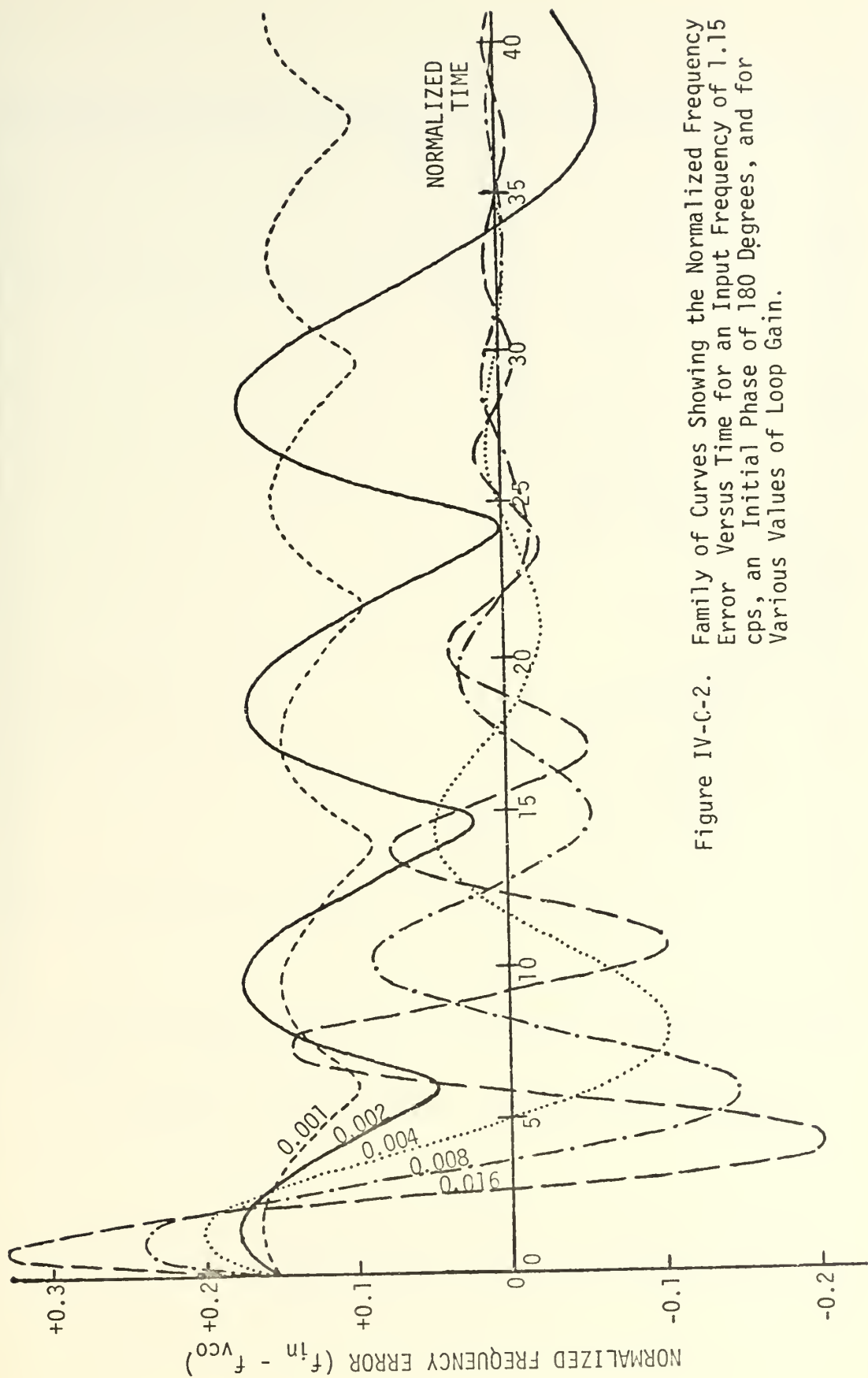


Figure IV-C-2. Family of Curves Showing the Normalized Frequency Error Versus Time for an Input Frequency of 1.15 cps, an Initial Phase of 180 Degrees, and for Various Values of Loop Gain.

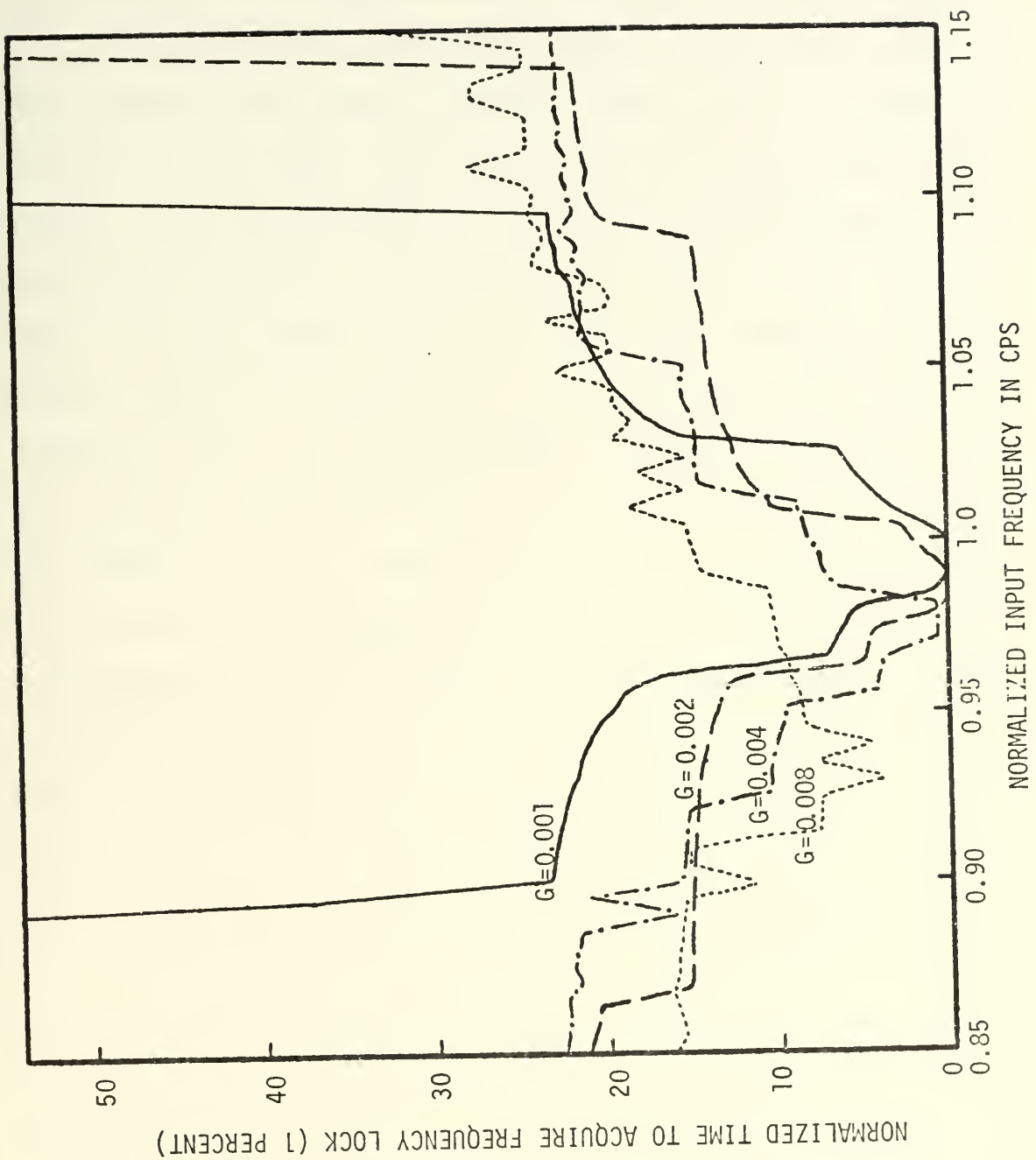


Figure IV-C-3. Frequency-Lock Time as a Function of Input Frequency for an Initial Phase of 180 Degrees and for Various Values of the System Gain.

the effects of starting phase, together with the fact that in this simulation the system began operating with the VCO pulse occurring first, overrides the effects of gain changes. Within this region, for input frequency higher than the VCO, the system attains lock faster for the lower value of gain. The frequency-lock times become even more erratic as the normalized gain is increased to 0.004 and 0.008, and it is no longer possible to make a general statement as to what value of gain will give the lowest lock time. This erratic behavior is due to several factors, one being that as the gain increases the system becomes more oscillatory, and therefore it becomes more difficult for the VCO to come within 1.0 percent of the input frequency. Another and more important factor is that for the particular type of phase comparator being studied the instantaneous frequency is always varying during each cycle, and as the normalized gain increases the instantaneous frequency variations increase also, which, together with the simulation techniques, begin to adversely affect the results. As the gain increases the system states change by greater amounts between computation time intervals, and therefore if realistic results are to be achieved the computation interval must be decreased by a factor proportional to that by which the gain was increased. This is particularly true in computing the average VCO frequency, where the average is computed by summing the value of the VCO frequency at each computation interval and dividing by the number of intervals during one period of the input signal. As the gain increases and the frequency varies significantly between intervals, the computed average VCO frequency also varies, and since frequency lock is based on the difference between the input frequency and the average VCO frequency, the computed lock times become unreliable. Due to computational time

limitations with the digital computer, it was impractical to decrease the computation interval sufficiently to study the effects of very high gains. However, the analog computer was used successfully with high gain values and its use will be discussed later.

Most of the digital simulation difficulties discussed above can be circumvented by changing the lock criterion from frequency lock to the phase-lock technique discussed in Subsection IV,B. The phase-lock criterion was used with a less stringent threshold, and it also avoided the difficulties involved in the computation of the average frequency. A family of curves giving the normalized time to attain phase lock as a function of the normalized input frequency is shown in Figure IV-C-4 for the same values of gain used in Figure IV-C-3. The phase-lock curves demonstrate a more predictable performance with changes in the normalized loop gain, and give a better indication of system operation independent of simulation techniques. Experimentation in changing the lock threshold resulted in changes to some of the values shown in both Figures IV-C-3 and IV-C-4, but the overall pattern was not affected significantly.

In order to avoid some of the difficulties encountered with discrete digital simulation techniques, the phase-locked loop's performance for high values of loop gain was studied using the analog computer simulation. Figure IV-C-5 shows the frequency-lock time as a function of gain for large values of gain and for several values of input frequency. The use of larger input frequency deviation was possible in the analog simulation because of the higher values of gain which were being used, thereby increasing the frequency range throughout which lock could be attained within reasonable computation time limitations. It can be observed in Figure IV-C-5 that for each frequency there is a certain

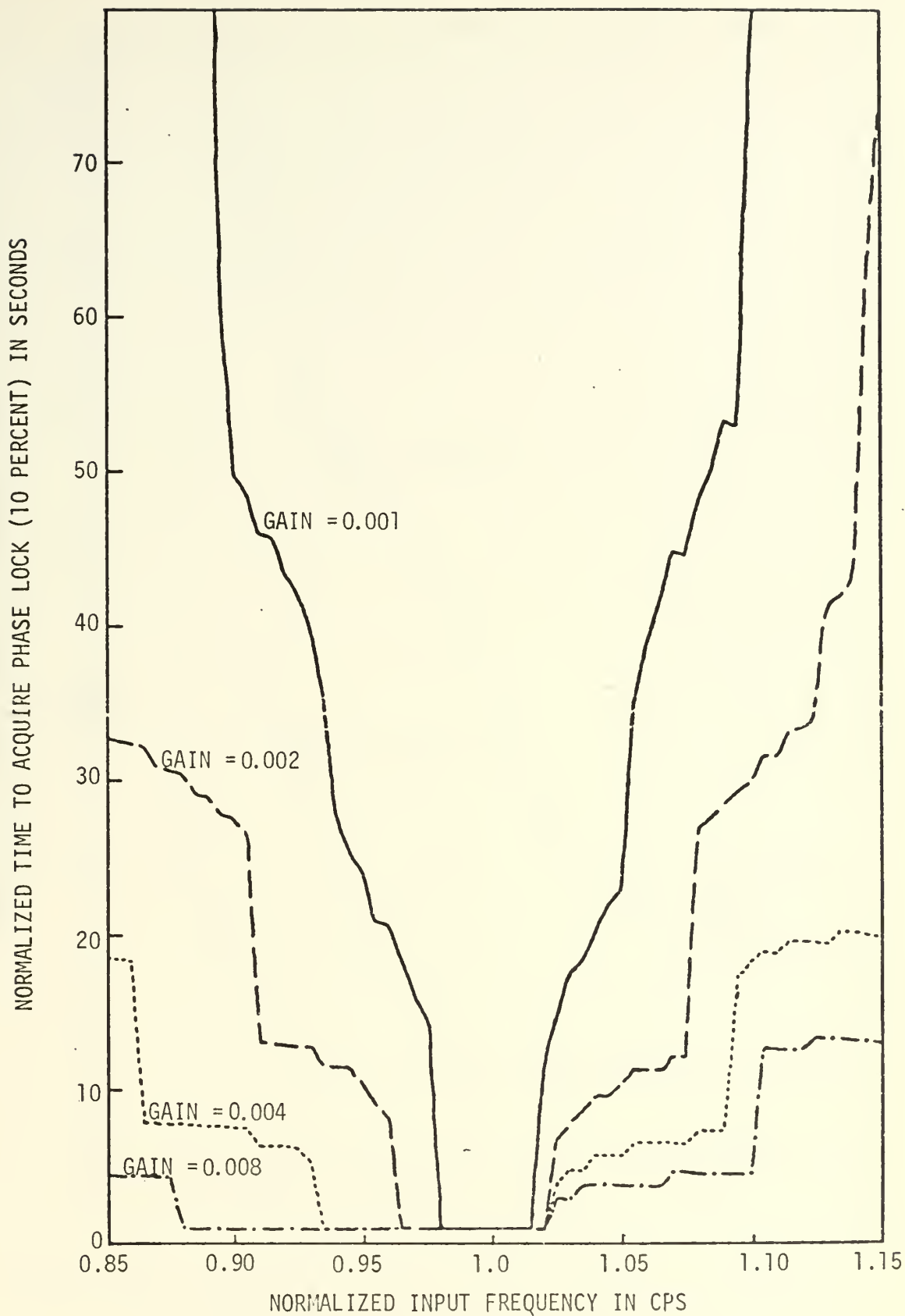


Figure IV-C-4. Normalized Time to Acquire Phase Lock as a Function of Normalized Input Frequency for Various Values of Gain and for ϕ_0 of 180 Degrees.

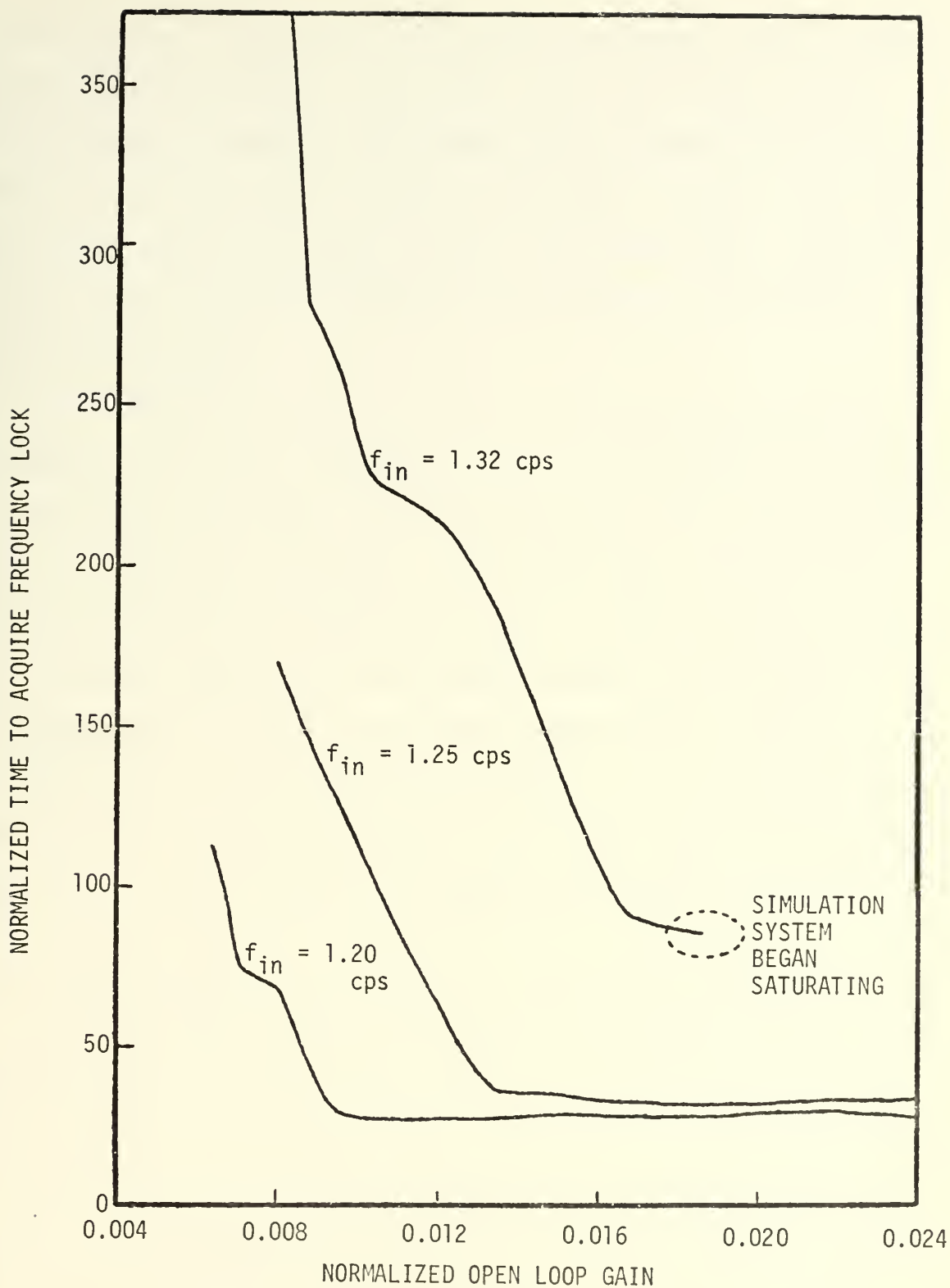


Figure IV-C-5. Analog Simulation Data of Frequency-Lock Time as a Function of Open Loop Gain, Using an Initial Phase of 180 Degrees and Several Values of Input Frequency.

threshold value of gain beyond which further increases in gain do not cause appreciable changes in lock time. This is the value of gain which drives the system to lock without cycle skipping, and the presence of this threshold gain can also be observed in Figure IV-C-2 for the digital simulation, where for gain values greater than a specific value no cycle skipping occurred and the system lock time remained relatively constant.

In the analog simulation the limits of maximum gain and maximum frequency deviation were determined, not by the characteristics inherent to the system under study, but by the saturation limits of the amplifiers used in the computer simulation. The increased lock range with high gain was accompanied by additional changes in system performance such as a decreased capability of the system to smooth out the jitter in an input pulse train, and other performance characteristics which are commensurate with increased bandwidth. Thus, as seen from the graphs presented in this section, the phase-locked loop responds to changes in loop gain in a manner typical to conventional feedback systems.

D. SYSTEM PERFORMANCE AS A FUNCTION OF FILTER CHARACTERISTICS

In all previous simulations the filter zero and pole were held fixed at the normalized values of 0.025 cps and 0.25 cps respectively, with only the gain and initial conditions of frequency and phase being changed. These values of the original lead-lag compensator had been based on a typical feedback compensator design using one decade separation between the pole and zero, which yields a positive phase angle of 55 degrees, and in this third order Type 2 system it also gives a phase margin ϕ_m of 55 degrees. In this section the effects of changing the compensator network will be studied.

The first step will be to investigate the consequences of varying the filter pole while maintaining the zero and system gain unchanged. From Figure III-A-5 it can be seen that if only the compensator pole is changed, the gain cross-over point will not be affected much except when the pole is placed very near the crossover. However, the phase margin and closed-loop bandwidth will be modified. Figure IV-D-1 shows the variation of phase margin and closed-loop bandwidth as a function of pole location. The digital simulation was used to obtain the plot shown in Figure IV-D-2 of the average frequency error ($f_{in} - f_{vco}$) as a function of time starting with a curve for the normalized pole at 0.065 cps and showing five additional curves, each curve for an increase of one octave in the pole location.

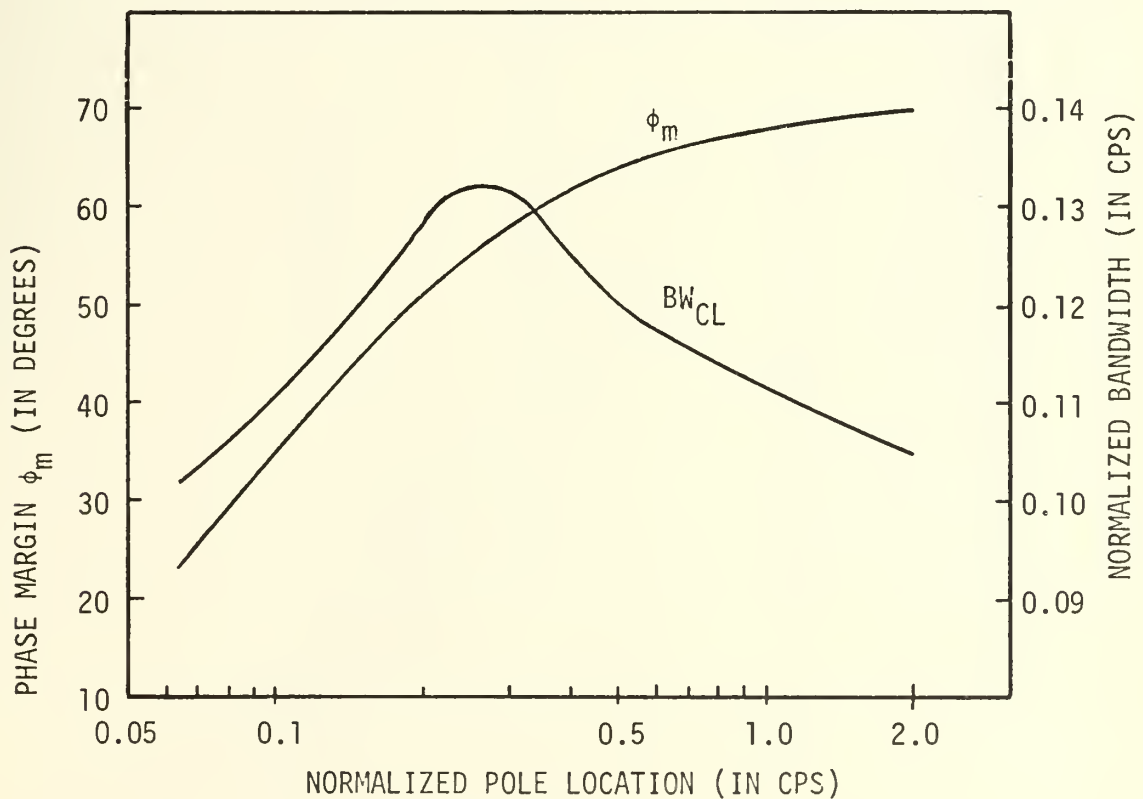


Figure IV-D-1. Normalized Phase Margin and Closed Loop Bandwidth as a Function of the Filter Pole Location.

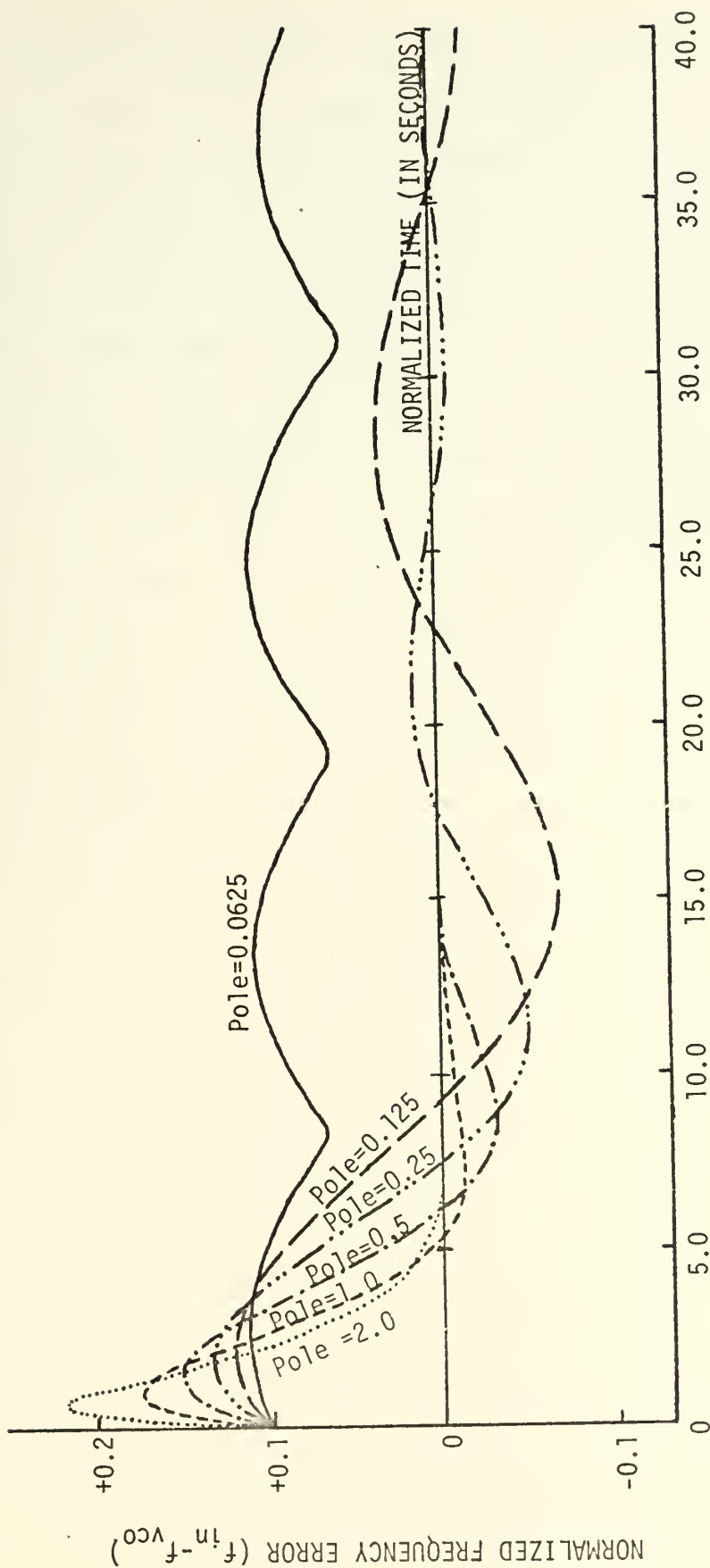


Figure IV-D-2. Normalized Frequency Error as a Function of Time for an Input Frequency of 1.1 cps, ϕ_0 of 90 Degrees, Gain of 0.002, and for Various Values of the Compensator Pole Location.

Figure IV-D-1 shows that as the pole is increased the phase margin is also increased, with ϕ_m approaching 90 degrees in the limit. This is also demonstrated in Figure IV-D-2 where the damping increases with the pole location until at a pole value of 2.0 cps the system is critically damped. However, the phase margin is not the only factor that is affected, and Figure IV-D-2 shows changes in performance which cannot be accounted for by changes in phase margin alone, nor can these variations be attributed to the changes in system bandwidth, since across the region of pole variations studied the bandwidth is only changed by a factor of 1.3. Furthermore, the changes in bandwidth are almost symmetrical about the 0.25 pole location, and Figure IV-D-2 shows a consistent change in the curves as the pole increases. The factor not yet considered and the one which accounts for these modifications of the curves is the effective change in the system gain due to the lead-lag compensator. The compensator zero causes the magnitude curve to increase with frequency at a rate of 6 db per octave until the frequency of the pole is reached. The resultant system gain at high frequencies has therefore been increased by 6 db for every octave of separation between the compensator pole and zero. The increase in the high frequency gain for the six pole locations used for the curves of Figure IV-D-2 is shown in Table IV-D-1, and this change in gain is what accounts for the decreased lock times and increased maximum frequency deviation shown in Figure IV-D-2.

To further study the interaction of the system's gain and filter characteristics, a family of curves was obtained showing the normalized frequency-lock time as a function of system gain while holding the relative effects of the filter constant by shifting the filter

<u>POLE LOCATION (CPS)</u>	<u>INCREASE IN HIGH FREQUENCY GAIN</u>
0.0625	1.58
0.1250	2.24
0.2500	3.16
0.5000	4.47
1.0000	6.31
2.0000	8.91

Table IV-D-1. Increase in the System High Frequency Gain for Various Values of Compensator Pole Location with the Compensator Zero Held Fixed at 0.025 cps.

simultaneously with the gain. These curves are shown in Figure IV-D-3. In producing these curves a solution for frequency lock was found at the design value of gain and then the gain was increased by the factor K while the pole and zero were increased by the factor \sqrt{K} , thereby maintaining their relative position constant with respect to the gain crossover point. This procedure produced a curve where the phase margin was held constant for all gain values, while the closed-loop bandwidth increased by a factor \sqrt{K} for each increase in gain by the factor K . The above procedure was then repeated for other values of relative pole locations and phase margins. This family of curves shows the effect of increased gain and bandwidth in decreasing the lock time for a given value of phase margin, and also clearly demonstrates the effect of varying the pole location and phase margin for any fixed value of system gain.

It should be noted that Figure IV-D-2 was simply a different aspect of looking at a cross-sectional view of the data of Figure IV-D-3 for a fixed value of gain. The difference in format being that Figure IV-D-3 shows only the time at which frequency lock occurred, while Figure IV-D-2 shows the instantaneous variations in the actual average system frequency error as a function of time.

In conclusion it can be said that the phase-locked loop responds to filter variations much the same as the conventional feedback control system in regards to damping, overshoot, and settling time, which in phase-locked loop applications corresponds to lock time. However, the correlation between the two systems becomes more nebulous when the nonlinear phenomenon of cycle skipping occurs in the phase-locked loop.

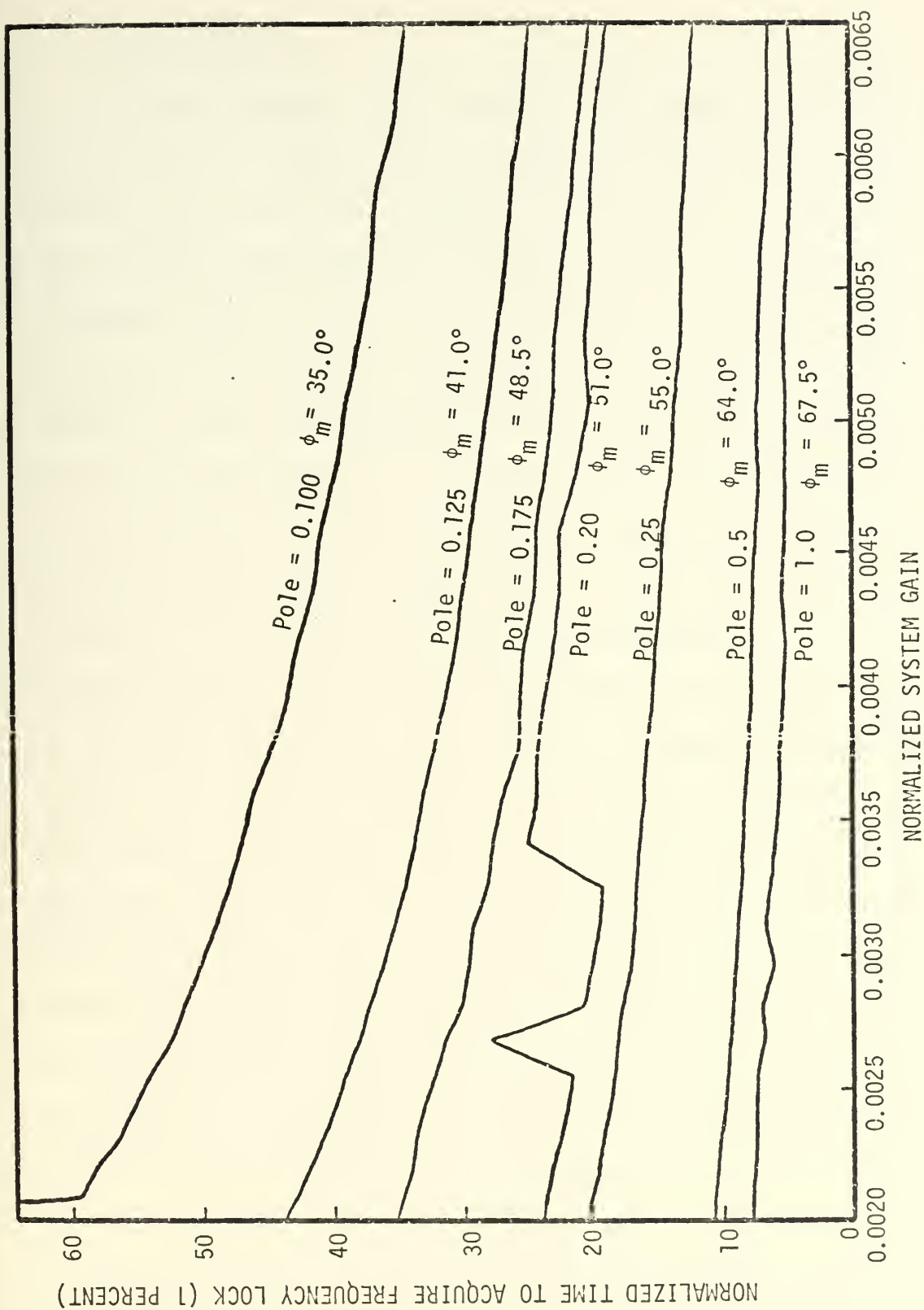


Figure IV-D-3. Normalized Time to Attain Frequency Lock as a Function of System Gain for a Normalized Input Frequency of 1.1 cps and ϕ_0 of 180 Degrees.

E. SEIZE FREQUENCY

The seize frequency f_s is defined as the highest f_{sh} and lowest f_{sl} value of input frequency for which the phase locked loop system will acquire lock without cycle skipping. The presence of a specific threshold frequency which separates the regions where cycle skipping occurs and where it does not occur has been previously demonstrated graphically in Figures IV-B-3 and IV-B-4 where the system performance as a function of time was shown for frequencies on either side of the seize frequency. Furthermore, the effects on the seize frequency have been previously observed in Figure IV-A-5 for variations of phase, in Figure IV-C-2 for variations of gain, and in Figure IV-D-2 for variations of the filter parameters. For all values of input frequency where $f_{sl} < f < f_{sh}$ the system performs as a linear system, and there are no sharp discontinuities in the system states except for the effects of sampling. The plots of Figures IV-A-4 and IV-B-1 which show lock times as a function of phase and frequency respectively, do show some jumps in lock times for frequencies which differ from the VCO by less than the seize frequency. However, a detailed study of these regions using plots of average VCO frequency as a function of time shows that these jumps in recorded lock times are due to the characteristics of the threshold detector used to determine lock, as discussed in Section III, and are not due to the presence of skipped cycles, as are the jumps in lock time which occur at the seize frequency.

In order to make a more detailed study of the seize frequency as a function of gain and phase, the digital computer simulation program was modified to detect the first occurrence of either two consecutive input pulses or two consecutive VCO pulses which indicated the presence of a

skipped cycle. An iterative procedure was then employed whereby the input frequency was varied either above or below the VCO frequency in broad steps until a frequency was reached where the system began skipping cycles. At this point a halving procedure was employed to take the two previous test frequencies, one which resulted in cycle skipping and one which did not, and then use their arithmetic mean as the next test frequency. This procedure was repeated until the difference between test frequencies became less than 0.0005. The resultant families of curves showing the seize frequency as a function of system gain for five values of the initial phase angle ϕ_0 are shown in Figures IV-E-1 and IV-E-2 for high and low frequencies respectively.

From Figures IV-E-1 and IV-E-2 it is seen that for all values of ϕ_0 the range of frequencies for which no cycle skipping occurs increases with gain. This can be easily understood from a physical point of view, since an increase of gain results in a greater corrective voltage being applied to the VCO and therefore the system is able to attain lock without cycle skipping for a greater initial frequency difference. The same reasoning serves to explain the increased spread between the curves of seize frequency for constant phase as a function of increasing gain for both high and low values of input frequency.

It can be observed in Figure IV-E-2 that the curves of seize frequency exhibit a steeper slope than the curves of Figure IV-E-1, indicating that the variation with gain is greater for low values of input frequency than for high values. This results from the fact that as the input frequency decreases, the period increases and thereby increases the period of time through which the VCO can act to integrate out the phase differences and attain lock. The system responds in just the opposite way for higher values of input frequency where increased gain results in increased

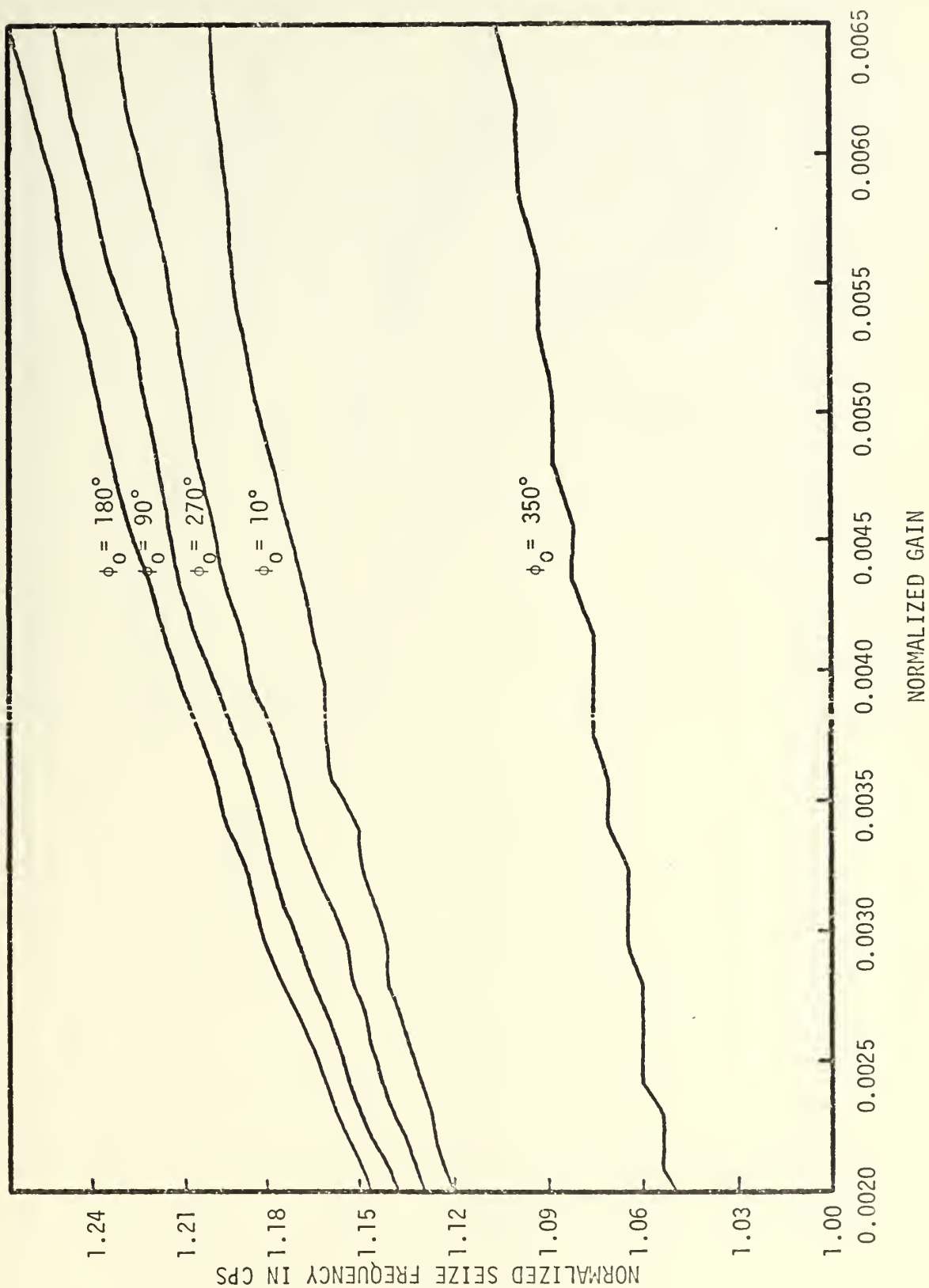


Figure IV-E-1. Normalized Upper Seize Frequency as a Function of Normalized Gain for Various Values of the Initial Phase Angle ϕ_0 .

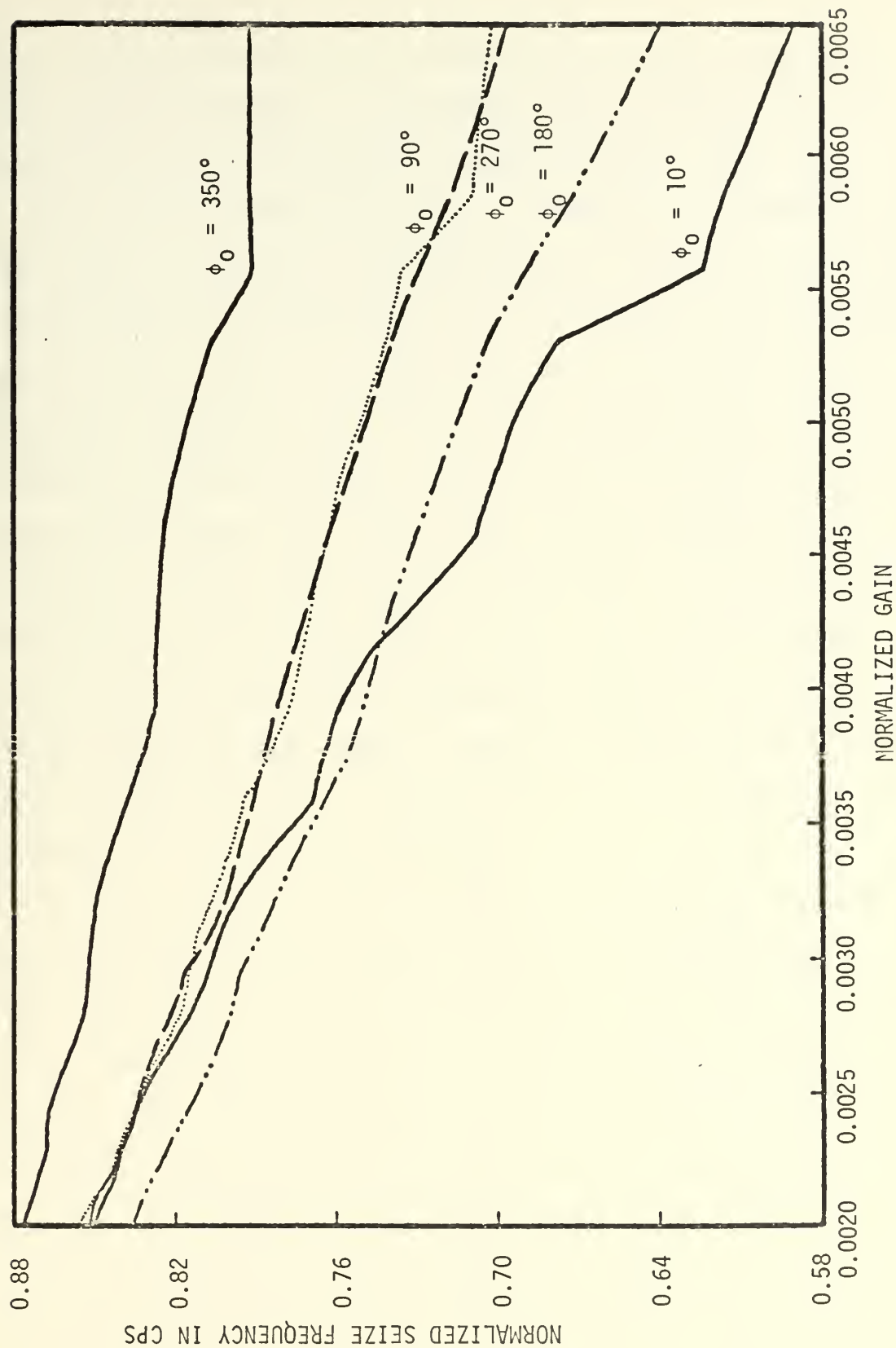


Figure IV-E-2. Normalized Lower Seize Frequency as a Function of Normalized Gain for Various Values of the Initial Phase Angle ϕ_0 .

values of seize frequency but shorter periods of time over which the VCO can cause adjustments. This explains why, in Figure IV-E-1, the slope of the curves decreases with increasing values of gain.

The variation of the normalized seize frequency as a function of the phase angle ϕ_0 by which the VCO lags the input is shown in Figure IV-E-3 for both high and low frequencies and for five values of the normalized open loop gain. Here it is seen again that the variation of seize frequency with phase is greater for the low frequencies than for the high frequencies, and the magnitude of the variation of the seize frequency from the VCO frequency for a given value of gain is greater for the low frequencies. Figure IV-E-3 shows a slightly wider variation of normalized gain than shown in Figures IV-E-1 and IV-E-2, and higher values of gain could have been displayed if the computation interval of the digital simulation had also been reduced. However, the values of normalized gain shown in Figure IV-E-3 more than exceed the range of values which might be employed in a typical system design.

Both Figures IV-E-1 and IV-E-3 show that for $\phi_0 = 350$ degrees and for the input signal frequency greater than the VCO frequency there is a significant reduction in the seize frequency. Since a phase relationship of $\phi_0 = 350$ degrees results in a displacement in time of $1/36^{\text{th}}$ of a period, then for the free-running condition where the VCO does not change in frequency the maximum value of normalized input frequency which could be applied to the system without causing cycle skipping within the first cycle would be 1.0286 cps. With feedback connected, the VCO changes frequency and the seize frequency increases; however, the time over which the VCO can act before a cycle is skipped is very short, and therefore for high values of ϕ_0 the seize frequency for input frequencies higher than the VCO tends to be very low. In general, the curves for seize

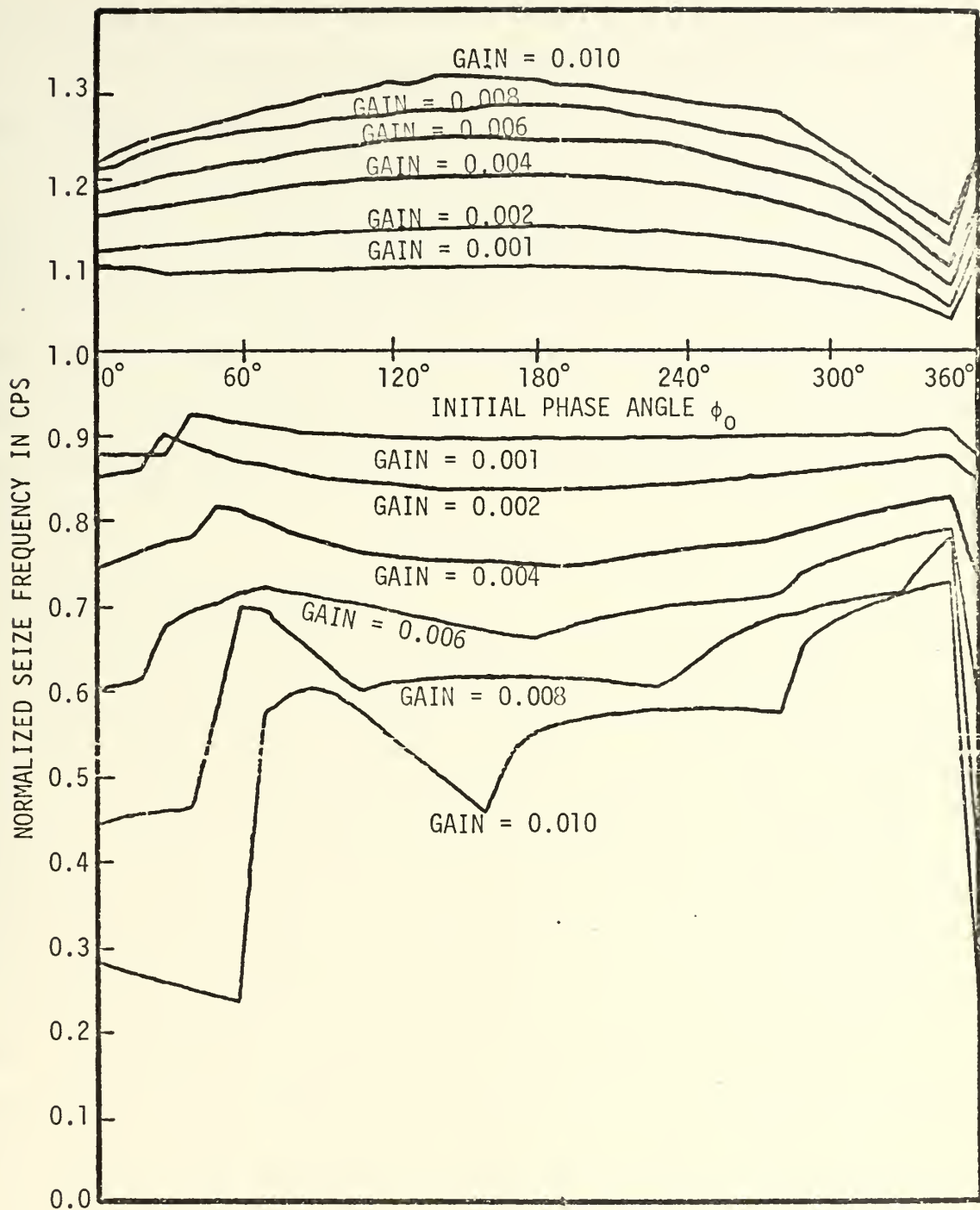


Figure IV-E-3. Upper and Lower Normalized Seize Frequencies as Function of the Initial Phase Angle for Various Values of the Normalized Loop Gain.

frequency as a function of phase are the most uniform in the region around $\phi_0 = 180$ degrees, and the curves exhibit variations near both the high and low values of ϕ_0 .

In summary it can be said that the deviation of the seize frequency from the VCO free-running frequency increases with an increase of gain, and that the deviation is greater for lower values of seize frequency than it is for higher values. In the particular system under study the limitation on the upper value of gain used was determined by the simulation techniques employed, and not by the characteristics of the system under study.

F. STEADY STATE PHASE ERROR

Using linear feedback control theory, as summarized in Table II-A-I, it was determined that the steady state phase error for a Type 2, third order system with a constant frequency input should be zero. Experimental results using both the analog and digital simulations confirmed this theory and revealed that in all cases, once the cycle skipping has ceased, the system would attain phase lock and, after a period of time required for the system to settle out, the phase error would also be reduced to zero. The amount of time required to attain zero phase error was a function of the system gain, with shorter times resulting from increased gain. However, the ultimate achievement of zero phase error was not dependent upon the gain and was a characteristic of the particular system under study. Thus, in regards to steady state phase error the system ultimately conformed to linear theory in spite of the nonlinearity of the phase comparator and the sampled-data characteristics introduced into the system by the use of pulsed waveforms.

G. LIMIT OF STABILITY

The Bode plot of the system open-loop transfer function given in Figure III-A-5 shows that if the phase-locked loop system under study is approximated by a continuous system, then stability is always guaranteed regardless of how large the loop gain is made. However, as mentioned previously there is a sampling effect that is inherent to the system operation, and which must be considered in any detailed evaluation of the system performance. The sampling effect is a result of the operation of the phase comparator whereby the output of the phase comparator applies either a positive or negative corrective voltage of constant amplitude to drive the system. At the occurrence of a pulse from the input signal waveform the control voltage is switched to its full positive value and maintained at that level causing the system to operate in an open loop condition until the occurrence of the VCO pulse which reverses the control voltage to its full negative value. Therefore, the phase comparator acts somewhat in the manner of a sample and hold circuit except that a sample and hold circuit is usually used to sample the amplitude of a waveform and retain the value of the sample, acting as an open loop circuit, until the arrival of the next sample. The phase comparator takes a single bit of information, which is the time of arrival of a pulse and not an amplitude function; and, just like in the sample and hold circuit, the most recent bit of information is used to supply the circuit with a fixed drive until the arrival of the next bit of information, which is the arrival of another waveform pulse. The quantity being sampled here is a time relationship and there is no real fixed sampling period, although there must be one sample from the VCO signal and one sample from the input pulse train during each period of the input signal except for those

periods during which a cycle is skipped by the VCO. These two samples or bits of information may occur very close together in time or they may occur widely separated in time. The fact should also be realized that the arrival of an individual pulse conveys no meaning whatsoever about the phase relationship since it takes a minimum of two pulses, one from each of the input and VCO signal waveforms, to determine the relative phase of the two signals. Thus a true sample or indication of the phase relationship is obtained only once during each period of the input signal, and the information is obtained in segments or steps such that during part of the period the system is actually being driven in the wrong direction. The sampling effects of the particular phase comparator under study cannot be directly equated to the normal concept of a sample data system, although there is definitely a modified sampling and holding action taking place.

Just as the R-S phase comparator cannot be considered as a strictly conventional sample and hold system, so also it cannot be considered as a truly continuous system. The instantaneous output of the phase comparator which is used to drive the system is merely a positive or negative voltage of constant magnitude and is no measure of the phase relationship. It is only the average of the voltage taken over a complete period of the input waveform that provides an indication of what the phase was. There is also a time delay inherent in the operation of the phase comparator since the phase relationship is not known until after a complete period of the input signal, although the system had been acted upon by inputs throughout the entire period and had been receiving some information (right or wrong) throughout the entire period.

The incorporating of the sampled data effect into the simulation process has not been accomplished in previous research on phase-locked

loops, and the only mention of this phenomenon was made by L. F. Judd [Ref. 45] where the effects of the phase comparator had been equated to a delay. Judd's reasoning was that there was no useable information being conveyed to the system until the arrival of the second pulse to reset the flip-flop in the phase comparator. He further observed that the delay corresponding to a conventional sample and hold circuit was approximately $\frac{\pi}{2}$, and that therefore the delay in the phase comparator must be somewhere between zero and $\frac{\pi}{2}$. From this he assumed a delay value of $\frac{\pi}{4}$ for the circuit operation. Judd's commentary is the only reference made in the literature to the sampling effects of this particular phase comparator circuit. Nevertheless, it was felt that the phenomenon was sufficiently important to study further, and this was one of the primary reasons why the research work carried out for this treatise was done using an exact simulation of the system including the effects of the sampling process rather than using the more conventional simulation methods which merely approximate the phase-locked loop as a continuous system with the output of the sawtooth phase comparator being given simply by $K(\phi_{in} - \phi_{vco})$, thereby eliminating all the sampling effects and time delays of the phase comparator.

A complete discussion of the effects of sampling is given by Dr. G. J. Thaler in Chapter 11 of Ref. 57. In this chapter Dr. Thaler provides a derivation and graph showing the approximate transfer function for a sample and hold circuit. If this transfer function is applied as a corrective factor to the phase plot of the open-loop transfer function of the phase-locked loop under study, a corrected Bode diagram for various values of sampling frequency f_{sam} appears as shown in Figure IV-G-1. The curves for several increasing values of gain are also shown in Figure IV-G-1, although the gain curves in this figure have not been corrected for

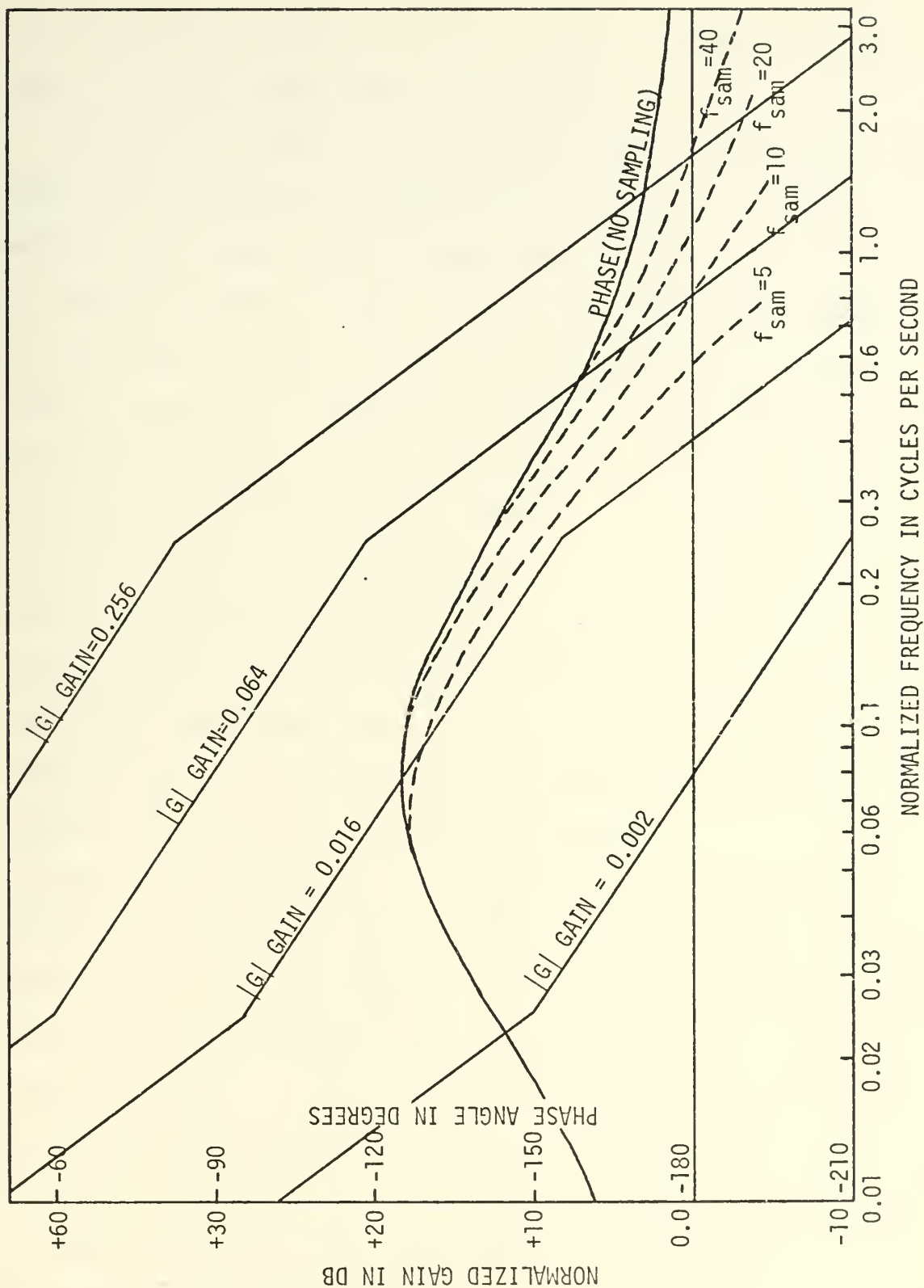


Figure IV-G-1. Bode Diagram for the Phase-Locked Loop System Showing the Phase Curve with Corrections Applied for Various Normalized Sampling Frequencies and Giving the Magnitude Curve for Large Values of Gain.

the sampling effect because the effect on gain is very slight, being less than one db in the region under consideration.

Figure IV-G-1 shows that if the sampling effects of the phase comparator could be equated to an equivalent sampling rate for a normal track and hold circuit then this equivalent sampling rate could be determined by the point at which a slight increase in gain would cause instability of the circuit. An effort was made to experimentally determine this point of instability by gradually increasing the gain while maintaining the filter parameters constant. Using the analog simulation the gain was increased to a value of 0.256 and the system continued to function correctly with the VCO quickly locking to the input signal and the steady state phase error being reduced to zero. Due to the high value of gain the instantaneous normalized frequency variations of the VCO within one cycle of the input signal became as great as 0.75 cps, but the system remained stable. Further increases in gain were prohibited due to limits on the operation of the simulation devices.

While the above experimental procedures did not give a clear answer as to the magnitude of the sampling effects, they did produce a limiting bound in that it has been determined that although explicit phase information is provided only once during the period of the input signal, the circuit configuration is such that this sampling has a net effect that is less than that of a conventional sample and hold circuit which operates at 40 times the input frequency. Thus, while the correct average value of the phase comparator output is not available until the end of the cycle, the average value is being accumulated throughout the cycle and the best estimate of the average at any given instant of time is constantly being utilized to control the phase-locked loop at that particular instant of time. Furthermore, this incomplete average which is being accumulated

has been shown to be quite effective in controlling the system; and, although the delay and sampling effect introduced into the system has not been determined exactly, it has been shown to be much less than the best estimate previously applied to the problem.

V. EVALUATION OF PHASE COMPARATOR CHARACTERISTICS

Throughout this discourse it has been stressed that the primary component which influences the operation of the entire circuit is the phase comparator. It is the phase comparator which contains the essential nonlinearities of the system, and it is the phase comparator which introduces the sample data phenomenon into the system performance. The remaining parts of the system such as the filter and the VCO are essentially linear components whose operating characteristics can be determined and are generally well known. It is therefore appropriate that the phase comparator characteristics undergo special study. In this section a comparative analysis will be conducted of several of the phase comparators which have been employed in phase-locked loops, and several new types of phase comparators will be proposed and investigated including an especially important nonlinear phase comparator. The operating characteristics of this nonlinear phase comparator have demonstrated improved performance over the phase comparators previously used in phase-locked loop applications, and have lead to increased frequency-lock-on ranges and reduced frequency-lock times. Some of the circuit variations discussed in this section have involved alternations which have not been made directly on the phase comparator but which have been designed to aid in studying phase comparator characteristics; and, because of their close connection with phase comparators, they have been included here instead of in a separate section.

Due to the large amount of data generated in this comparative analysis, it was impractical to include in this treatise all the data for each phase comparator which has been provided in the case of the R-S

phase comparator in Section IV. Instead, only those particular families of curves will be shown which demonstrate the way in which the specific phase comparator under study varies from that of the R-S or other phase comparators. In this way emphasis will be placed on the essential differences observed between the various phase comparators under study.

A. R-S PHASE COMPARATOR

The R-S phase comparator has been studied in detail in Section IV where curves have been given to show the system performance as a function of initial phase and frequency differences, gain, and filter characteristics. The seize frequency has also been studied as a function of both gain and phase, and it was seen that both the lock range and the stability range of the system using the R-S phase comparator were unlimited within the range of parameter values which could be studied experimentally using the simulation techniques available. One characteristic of the R-S phase comparator which has been seen previously in the analog computer results shown in Figure III-B-7, which deserves additional comment here, is the instantaneous frequency variation which is characteristic of this type of phase comparator. With the R-S phase comparator, even when the system is locked, there is always a control voltage being fed into the loop filter from the output of the phase comparator. This voltage has a constant magnitude but changes in polarity, being positive for one half the period of the input waveform and negative in the other half of the input period, thereby causing the filtered output to the VCO to vary in similar fashion. Since the system is operating as a linear circuit when in lock, the voltage to the VCO will be that of a filtered bipolar square wave. The instantaneous VCO frequency will follow its control voltage and will also oscillate from a high to a low value once during each cycle

of the input waveform. Therefore, although when in lock the average VCO frequency will exactly equal that of the input waveform, the instantaneous frequency output of the VCO may vary between wide limits. This situation is demonstrated in Figure V-A-1 where the digital simulation program was used to compute two curves, one showing the instantaneous frequency error $f_e = (f_{in} - f_{VCO})$, and the other showing the average frequency error f_{ea} where f_{ea} is the frequency difference averaged over one period of the input signal. It is seen that the average frequency error reduces to zero as the system locks and the transients settle out, but the instantaneous frequency error continues to vary even in the steady state condition. This continued variation of the VCO frequency might be undesirable and cause serious performance degradation for particular circuit applications, and for those applications it would be necessary to use one of the other phase comparators discussed later in this section which does not have the large instantaneous frequency variation. However, for applications which are only concerned with the phase relationships at a particular instant of time, the VCO variations discussed above might be immaterial since, as was pointed out earlier in Section IV, the circuit does operate effectively with zero steady state phase error.

One other aspect of the R-S phase comparators operation which should be considered is the effect on circuit operation of temporarily losing the input signal. This zero-input condition might take place at the beginning of circuit operation or at some time after steady state operation had been attained. In either case the R-S phase comparator will cause the circuit to quickly deviate from its normal VCO operating frequency to a very low frequency where component saturation will take place. This occurs because the loss of an input signal to the phase

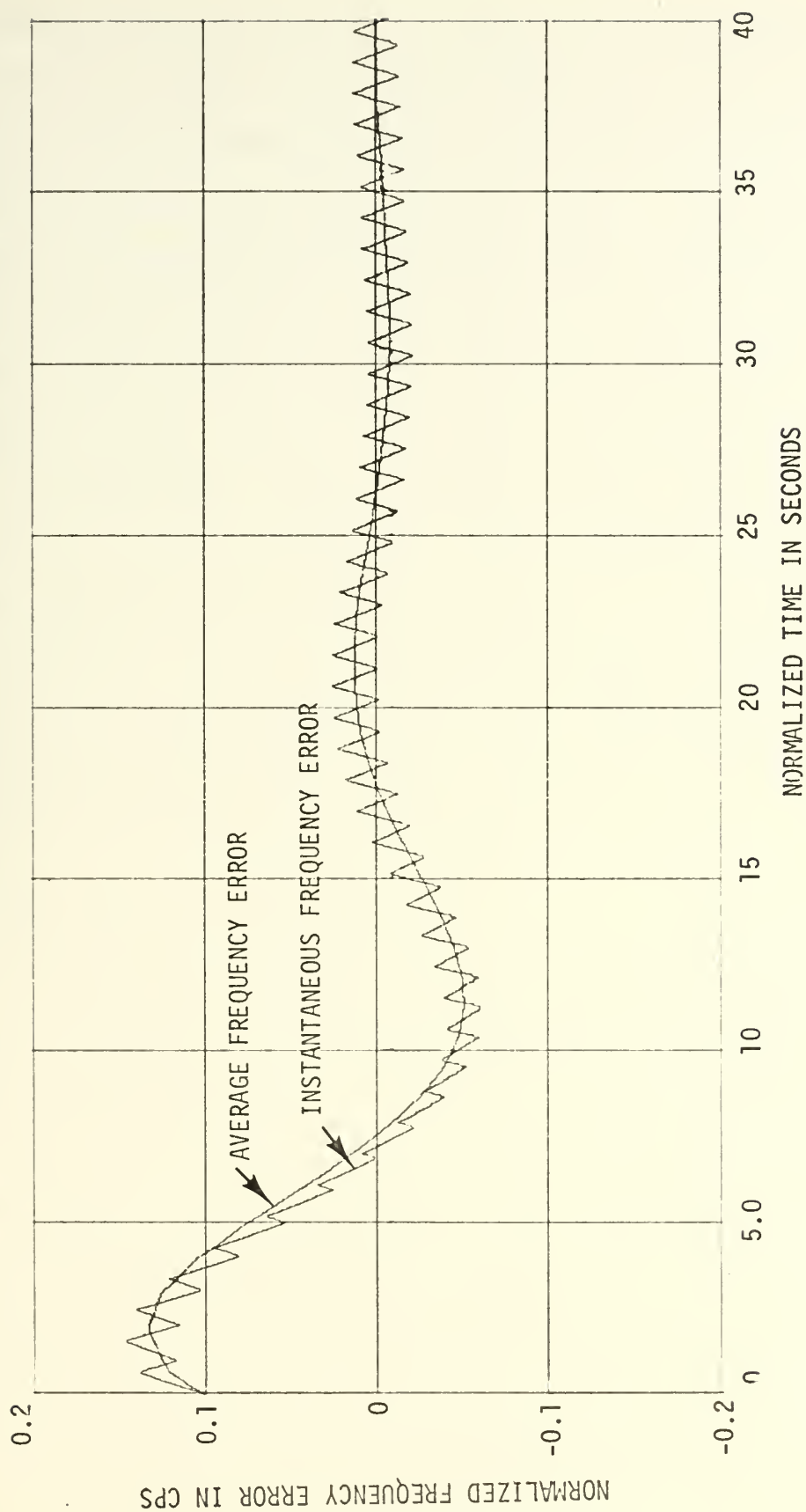


Figure V-A-1. Instantaneous and Average Normalized Frequency Error as a Function of Normalized Time for the Normal R-S Phase Comparator with a Gain of 0.002 and Initial Conditions of $f_{in} = 1.1$ cps and $\phi_0 = 90$ Degrees.

comparator forces the flip-flop to remain in the reset condition indefinitely, causing a constant amplitude negative voltage to be applied to the VCO through the filter and resulting in the VCO frequency being driven down to the lowest possible limits of its operation. As a result, this particular phase comparator would not be practical in cases where the input signal was intermittent or where a low signal to noise ratio existed, and in addition, this particular phase-locked loop circuit cannot be activated prior to the arrival of the input signal pulse train.

The complication resulting from the zero-input condition discussed above can be somewhat alleviated by applying the VCO signal to a 'count' input connection of the flip-flop, and then the VCO will continue to operate with no input at the same average frequency at which it was operating at the time the signal was lost. A modification to this technique is described more thoroughly in Section V, E below, where the operation of the trigger phase comparator is discussed.

B. NONLINEAR R-S PHASE COMPARATOR

Since the phase comparator is such an essential component of the phase-locked loop, it is a natural target for studies aimed at improving the system performance. It was revealed in Section III and demonstrated by Figure III-A-4 that one of the main advantages of the sawtooth phase comparator over the sine comparator was the increased control voltage which the sawtooth phase comparator generated for large phase variations. By expanding on this concept the experimenter is lead to the conclusion that the ideal phase comparator would be one which would generate a very large corrective voltage when a large phase error existed, and which would decrease the amount of the control voltage as the phase error decreased. In this way the system could quickly adjust to large phase errors and yet

the reduced small signal gain would prevent overreaction leading to excessive oscillation. This desirable phase characteristic curve would require the addition of another nonlinearity to an already nonlinear device. However, even this compounding of nonlinearities would be expedient if the net result were sufficiently advantageous.

Having determined the general characteristics of an ideal phase comparator, it was then necessary to formulate a specific method of implementation. The normal R-S phase comparator described previously was used as a basis, but now the output of the flip-flop was modified from a constant value output to an exponentially decaying voltage. Each time the flip-flop was either set or reset the voltage output began at a positive or negative amplitude denoted by AMP and decayed exponentially toward zero with a time constant TC. The operation of the R-S nonlinear phase comparator was as shown in Figure V-B-1.

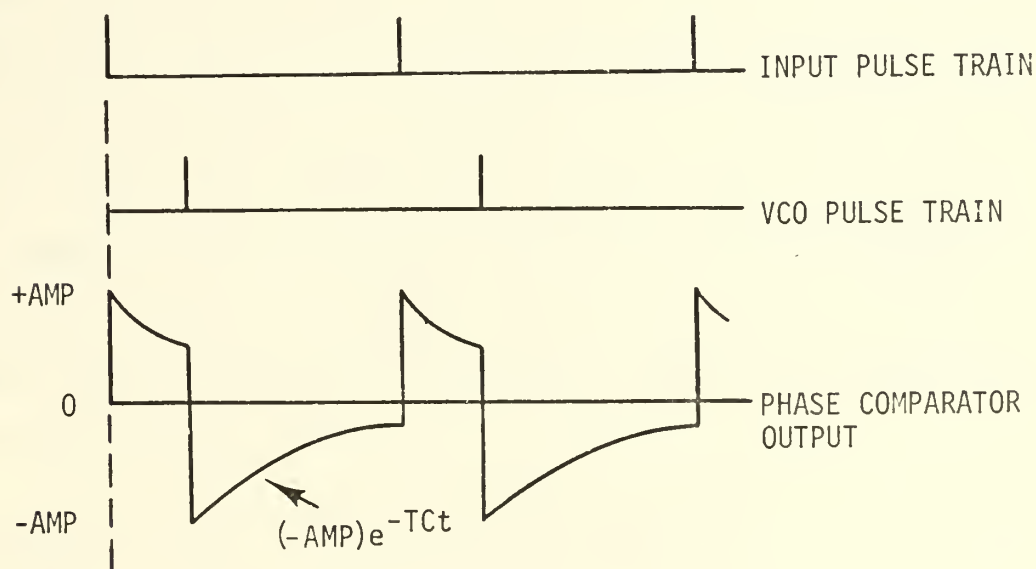


Figure V-B-1. Operation of the R-S Nonlinear Phase Comparator.

The equation for computing the average phase comparator output over one period of the input waveform as a function of the phase difference by which the VCO signal lags the input signal is given as

$$f(\phi_{on}) = \int_0^{\phi_{on}} AMP e^{-TCx} dx - \int_0^{1-\phi_{on}} AMP e^{-TCx} dx, \quad * \quad (V-b-1)$$

where ϕ_{on} is the phase angle normalized to unity and obtained by dividing the actual phase angle by 2π radians. The solution to Equation V-b-1 is given by

$$f(\phi_{on}) = \frac{AMP}{TC} \left(-e^{-TC\phi_{on}} + e^{-TC} e^{-TC\phi_{on}} \right) . \quad (V-b-2)$$

Equation V-b-2 contains two variable parameters, since both the amplitude and the time constant are independent quantities. However, a fixed relationship between these two parameters may be determined if a stipulation is added to the system concerning the steady state gain. This stipulation is that the nonlinear phase comparator is required to have the same steady state or small signal operating characteristics as that established for the original R-S phase comparator, and therefore its gain in the vicinity of $\phi_0 = 180$ degrees or $\phi_{on} = 0.5$ must be the same as that of the linear sawtooth phase comparator. The gain of the R-S phase comparator can be determined from Figure III-A-4 as $\frac{\Delta f(\phi_{on})}{\Delta \phi_{on}} = 2.0$. It was then necessary to determine the slope of the nonlinear phase comparator from its characteristic equation given in Equation V-b-2, and this slope was found to be

$$\frac{df(\phi_{on})}{d\phi_{on}} = AMP \left(e^{-TC\phi_{on}} + e^{-TC(1-\phi_{on})} \right) . \quad (V-b-3)$$

* This equation and the following four equations only apply when $f_{in}=1.0$, the generalized form for any input frequency is given later in Equation V-b-6.

The slope was then evaluated at the point $\phi_{on} = 0.5$ and found to be

$$\left. \frac{df(\phi_{on})}{d\phi_{on}} \right|_{\phi_{on}=0.5} = 2 \text{ AMP } e^{-\frac{TC}{2}} . \quad (V-b-4)$$

Setting Equation V-b-4 equal to 2.0, which is the slope of the R-S phase comparator, a relationship was established between AMP and TC which is given by

$$\text{AMP} = e^{\frac{TC}{2}} . \quad (V-b-5)$$

Equation V-b-5 must be satisfied in order for the nonlinear phase comparator to have the same small signal response as the conventional R-S phase comparator.

The digital computer was used to calculate and plot $f(\phi_{on})$ for six values of TC while always maintaining the relationship shown in Equation V-b-5. The phase comparator characteristic curves for the R-S nonlinear phase comparator utilizing various values of TC are shown in Figure V-B-2 together with the characteristic curve for the normal R-S phase comparator used in all previous experimental work of this treatise. From Figure V-B-2 it can be seen that all the nonlinear phase comparator curves do have the same slope as the normal R-S phase comparator for small variations from the steady state phase relationship. However, for large phase variations the nonlinear response curves are designed to generate a much larger corrective voltage, and thus improve the lock-on characteristics of the system. From Figure V-B-2 it is seen that for greater values of the time constant the initial voltage decays more quickly, and therefore if the small signal gain is to remain constant the initial amplitude is required to be greater. The larger initial amplitude then causes the nonlinear curves to deviate further from the normal R-S curve at the extreme values of phase for larger values of TC than for smaller values of TC.

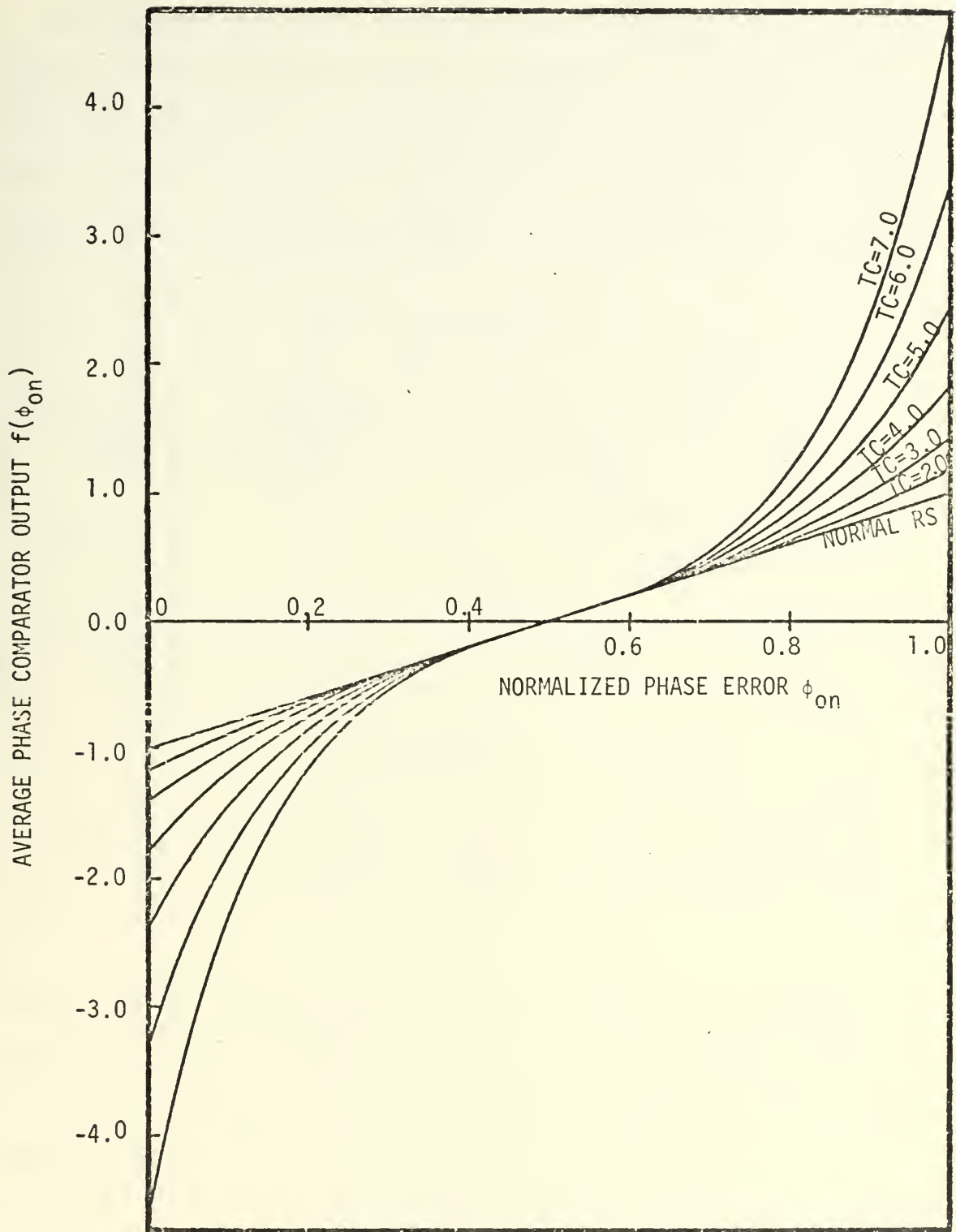


Figure V-B-2. Characteristic Curves of the R-S Nonlinear Phase Comparator for Various Values of the Time Constant Together with the Characteristic Curve of the Normal R-S Phase Comparator.

The R-S nonlinear phase comparator was incorporated into the analog computer simulation by inserting an R-C network at the output of the regular R-S flip-flop. Figure V-B-3 shows how the analog phase comparator circuit of Figure III-B-4 appeared after the inclusion of the RC network in both the normal and inverted outputs of the R-S flip-flop.

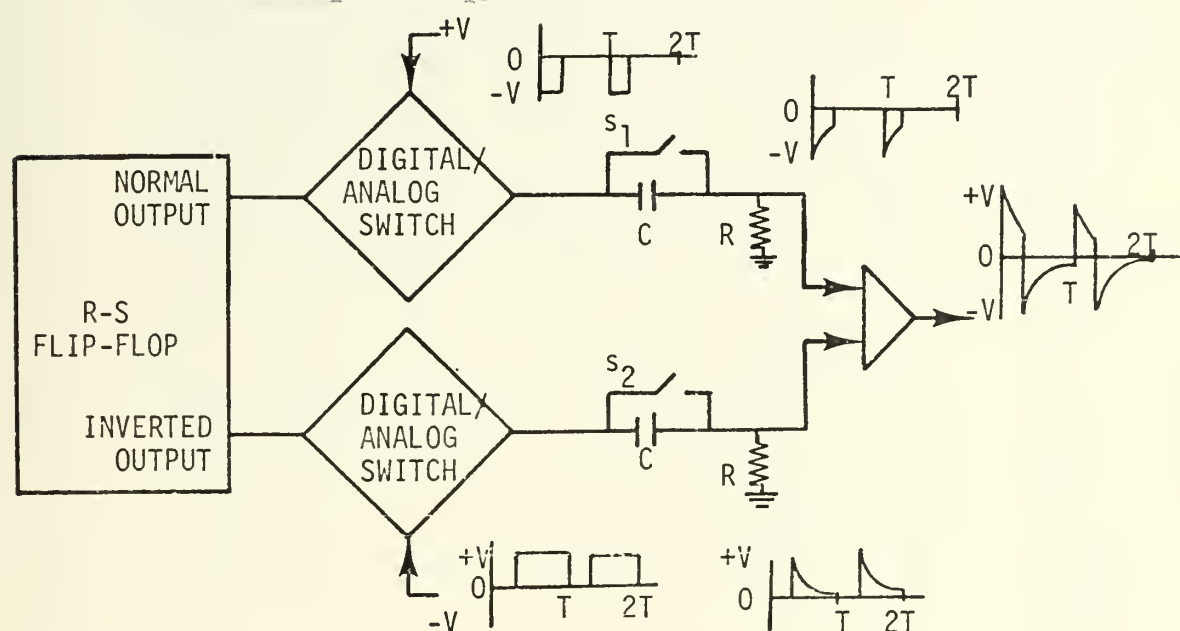


Figure V-B-3. Analog Phase Comparator Circuit After Being Modified to Develop a Nonlinear Output.

The addition of the relay across the capacitors of the RC networks was required in order to establish the proper initial conditions, and both S1 and S2 were controlled by voltages from the R-S flip-flop so that the switches were closed at all times when no signal was present at the output of the digital/analog switch. The initial amplitude was controlled by a potentiometer setting, and the time constant was controlled by the selection of the proper values of the resistor and capacitor in the RC network. The operation of the analog phase comparator is shown in Figure V-B-4 where both the input signal pulses (long pulses) and the

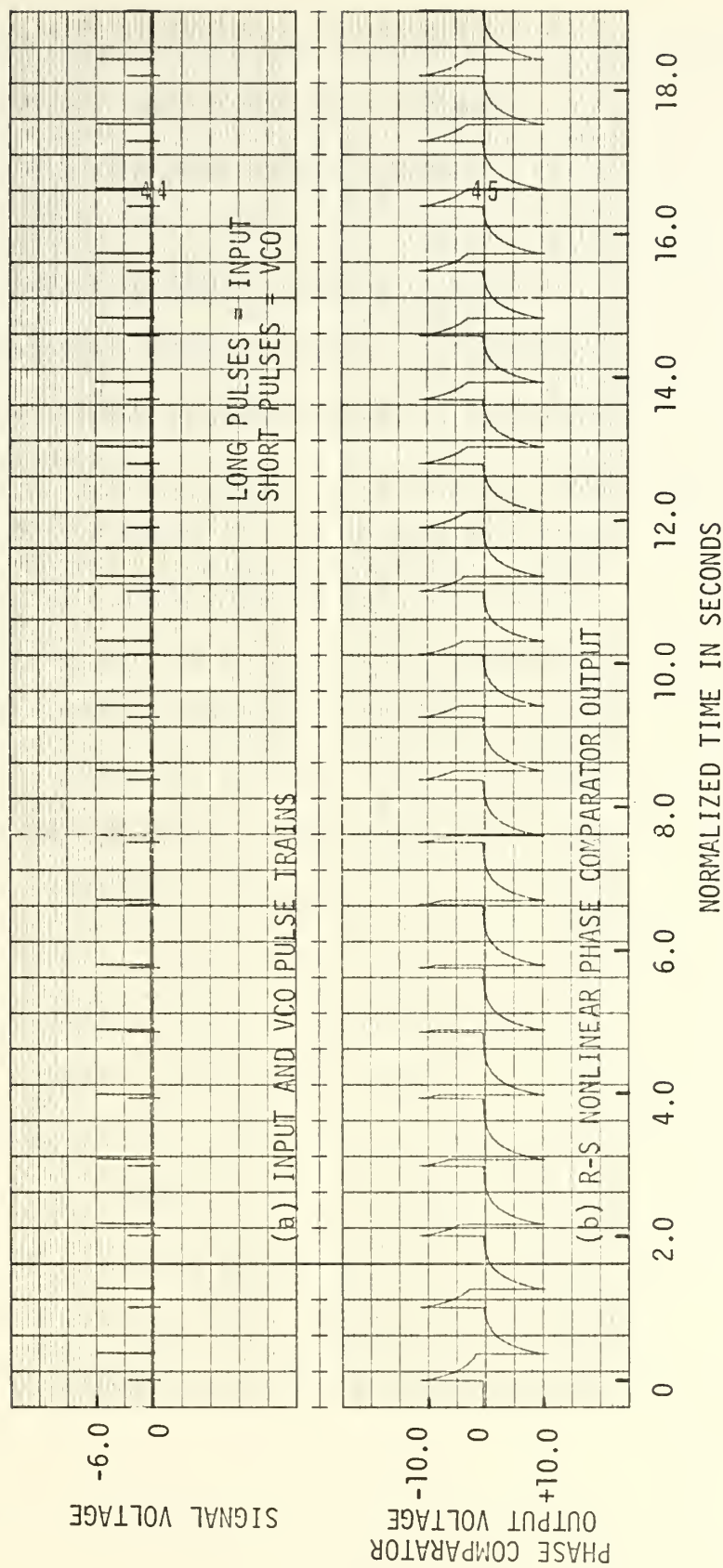


Figure V-B-4. Input and Output Waveforms of the Analog R-S Nonlinear Phase Comparator.

VCO pulses (short pulses) are shown on one recorder channel, with the corresponding output of the phase comparator for $TC = 5.0$ and $AMP = 12.18$ shown on the other recorder channel. The normal R-S phase comparator output with the same small signal gain was simply a one volt constant amplitude pulse switching between positive and negative values.

The nonlinear phase comparator was added to the digital simulation program by zeroing a timer function at the occurrence of each pulse from either the input signal or the VCO, and then incrementing this timer function by the amount DT , the integration interval, at each computation interval. This timer function was then used during each time interval to compute the current value of the exponential output of the phase comparator using the parameters of AMP and TC which were specified for that run. For the R-S nonlinear phase comparator the analog computer was again used primarily in the experimental stage to check out new theories and concepts. After the circuit checkout was completed, the digital computer simulation was used to collect the majority of the data and to obtain curves of operating characteristics due to the digital computer's greater convenience in obtaining large amounts of data.

A family of curves showing the normalized average frequency error as a function of normalized time for various values of the phase comparator time constant is shown in Figure V-B-5. In this figure the gain was held constant at its nominal value of 0.002 , and here, as in all other work of this treatise involving the nonlinear phase comparator, only the time constant was specified since the amplitude was made to relate to the time constant by Equation V-b-5. It can easily be seen from Figure V-B-5 that for the set of initial conditions given, the lock time is significantly reduced as the time constant is increased. In fact, the frequency lock time was decreased to as little as one half of its original value as

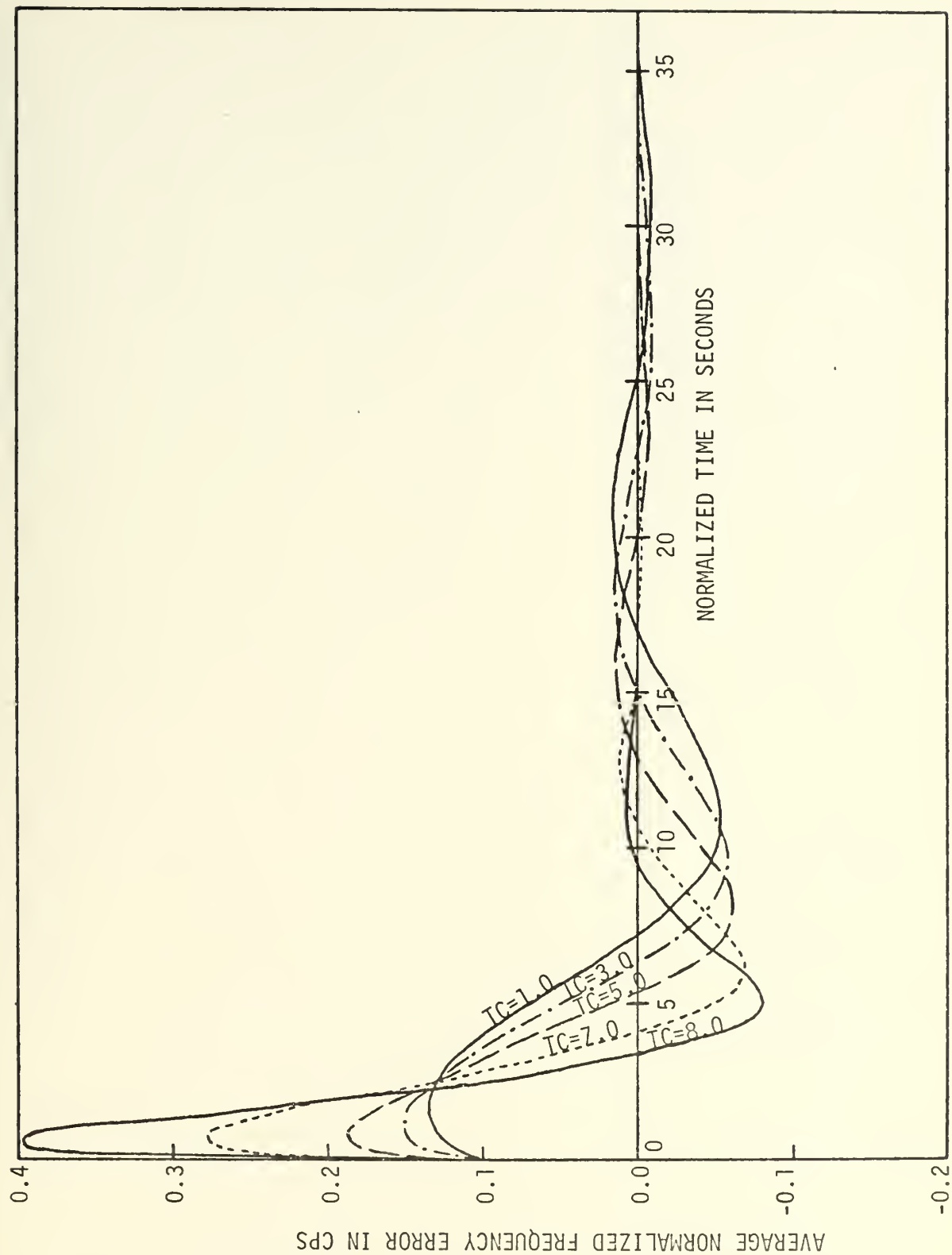


Figure V-B-5. Normalized Average Frequency Error as a Function of Normalized Time for the R-S Nonlinear Phase Comparator with a Gain of 0.002, an Input Frequency of 1.1 cps, an Initial Phase of 90 Degrees, and for Various Values of the Nonlinear Time Constant.

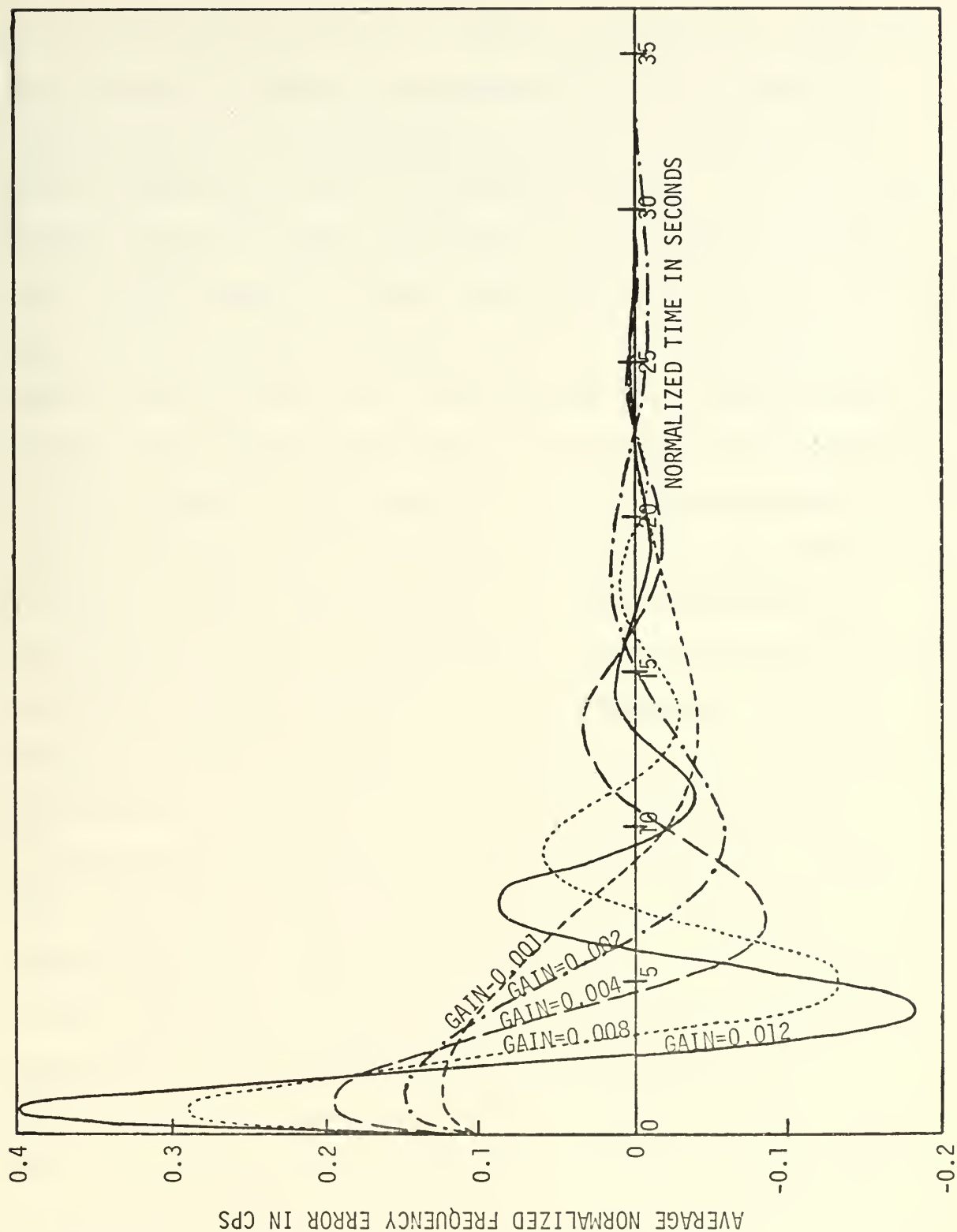


Figure V-B-6. Normalized Average Frequency Error as a Function of Normalized Time for the R-S Nonlinear Phase Comparator with a Time Constant of 3.0, Input Frequency of 1.1 cps, Initial Phase of 90 Degrees, and for Various Values of Gain.

TC was increased from 1.0 to 8.0. However, along with the reduced lock time there was an increase in the peak overshoot as the system first began operation. This increased peak overshoot is indicative of a highly increased gain, but an increased gain results in not only a large initial overshoot but also a large second and third overshoot together with a lightly damped oscillation. These later characteristics of a high gain circuit are missing in the curves for the R-S nonlinear phase comparator shown in Figure V-B-5. Of course some of the high gain characteristics were expected to be missing, since the nonlinear phase comparator was designed to have a large gain only for large phase errors, and then the system gain would automatically be reduced to the normal value of 0.002 as the phase error decreased. To further demonstrate this point consider the family of curves shown in Figure V-B-6 where again the normalized average frequency error is shown plotted as a function of normalized time, but for these curves the time constant was held fixed at a relatively low value of 3.0 with the loop gain being varied.

In comparing the data shown in Figures V-B-5 and V-B-6 it is seen that approximately the same amount of initial overshoot occurs for the operating condition of gain = 0.002 with TC = 8.0, or for the condition of gain = 0.012 with TC = 3.0. There was a significant difference between the two curves though in that the curve obtained by using the larger value of gain was more oscillatory and the oscillations did not damp out as quickly as for the curve obtained for the system which used a lower value of gain and a higher value of the time constant. In effect the nonlinear phase comparator has given the system the advantage of a high gain without the oscillations which usually accompany such a high gain, and in this way the lock times have been reduced. The curves of Figures V-B-6 still damp out much more quickly than the corresponding

curves for the normal R-S phase comparator and therefore still result in reduced lock times, but as the loop gain is increased the effects of a small nonlinearity tend to become masked by the effects of the large gain. The curves of Figure V-B-6 also show that the system with the R-S nonlinear phase comparator remains stable with increasing gain. In fact, further experimentation carried out on the analog computer indicated that the system was stable for all values of increasing gain within the limits of the simulation system's performance capabilities.

The relationship between frequency-lock times and the initial phase angle for the R-S nonlinear phase comparator was studied using the digital simulation, and Figure V-B-7 contains three curves showing how the frequency-lock time varies as a function of phase for three different values of normalized input frequency with a time constant of 5.0 and a gain of 0.002. In comparing the data of Figure V-B-7 with that of Figure IV-A-4, which shows similar gain and input frequency conditions obtained by utilizing the normal R-S phase comparator, it can be seen that the lock times for the R-S nonlinear phase comparator are significantly less than those of the normal R-S phase comparator. In fact the average lock time of the R-S nonlinear phase comparator is only one half to two thirds that of the normal R-S phase comparator. The most significant difference between the curves of Figures V-B-7 and IV-A-4 occurs towards the edges of the figures where the initial phase difference varies by a large amount from the steady state phase value. It is in these regions that the nonlinear phase comparator has its greatest advantage because here, as seen in Figure V-B-2, the largest corrective voltage is generated. Another observation that can be made is that for zero frequency offset there is a region within 40 degrees of the steady state phase position where the frequency-lock times for the normal R-S

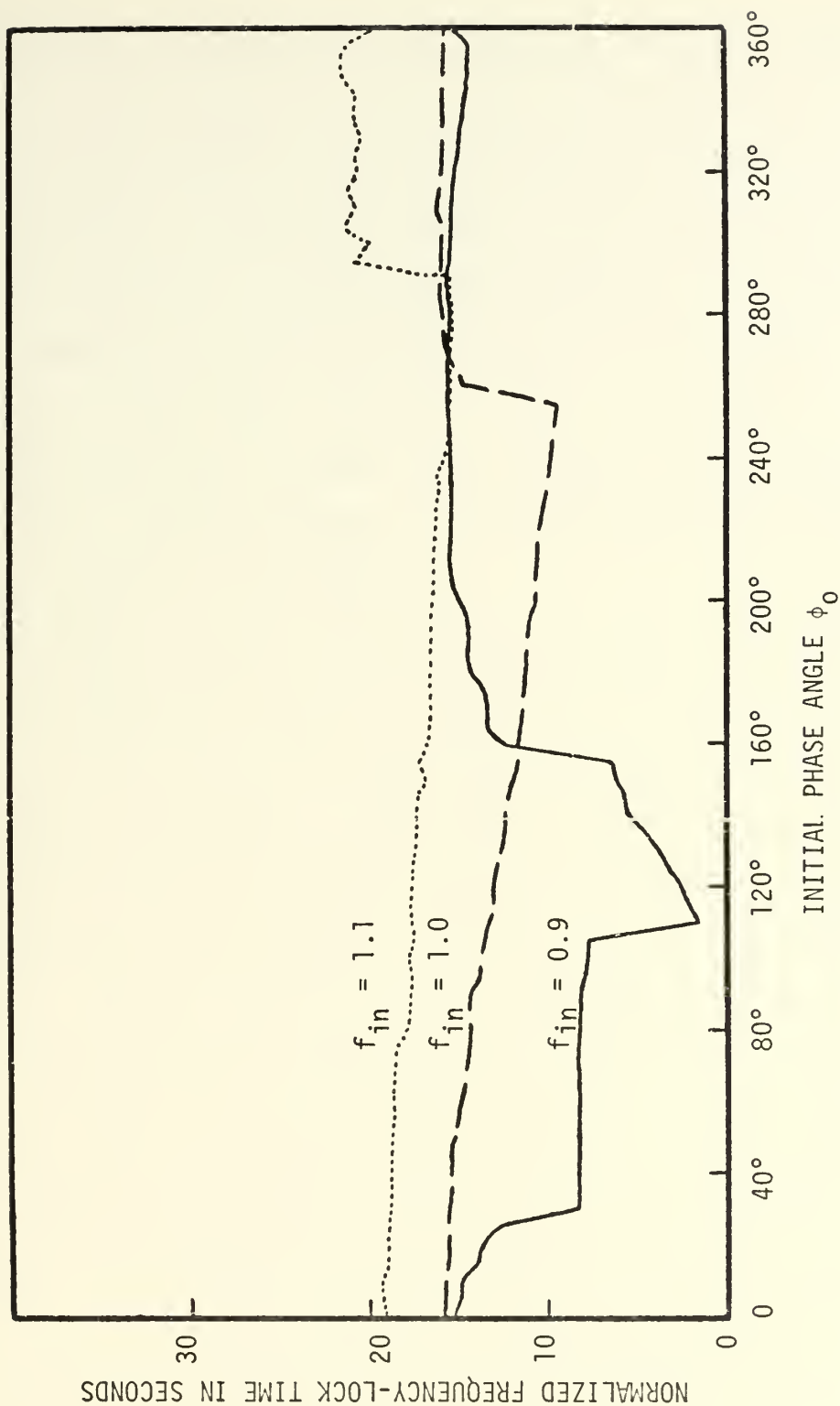


Figure V-B-7. Frequency-Lock Time as a Function of Initial Phase for the R-S Nonlinear Phase Comparator with a Gain of 0.002, TC of 5.0, and for Various Values of Input Frequency.

phase comparator are actually less than the corresponding times for the nonlinear phase comparator. This is the region where the initial conditions on both frequency and phase are such that the system is essentially at its steady state operating conditions from the beginning, and the greater variations in instantaneous VCO frequency caused by the nonlinear phase comparator result in a diminished stability and yield slightly longer lock times in this region. In effect, the addition of the nonlinearity has served to equalize the lock times over the entire range of input phase, with the average value being significantly less than that of the normal R-S phase comparator.

The digital computer simulation was also used to study the variation of the frequency-lock time as a function of the input frequency, and Figure V-B-8 contains curves showing this variation for three values of the initial phase angle. A comparison of Figure V-B-8 with Figure IV-B-1 shows that for an initial phase angle of either 270 or 90 degrees, the R-S nonlinear phase comparator resulted in significantly reduced lock times. This was especially true for input frequencies which differed by more than 5 percent from the free-running VCO frequency. The curve in Figure V-B-8 which portrays the lock times for an initial phase angle of 180 degrees indicates that the lock times for the R-S nonlinear phase comparator are also less than that of the normal R-S phase comparator, but for this curve there exists a region very near the VCO center frequency for which the normal R-S phase comparator attains lock quicker than the nonlinear phase comparator. This is the same phenomenon which has been discussed previously in connection with Figure V-B-7.

Additional data has been taken to investigate the variation of lock time as a function of frequency for initial phase angles other than those shown in Figure V-B-8. The differences between the normal R-S phase

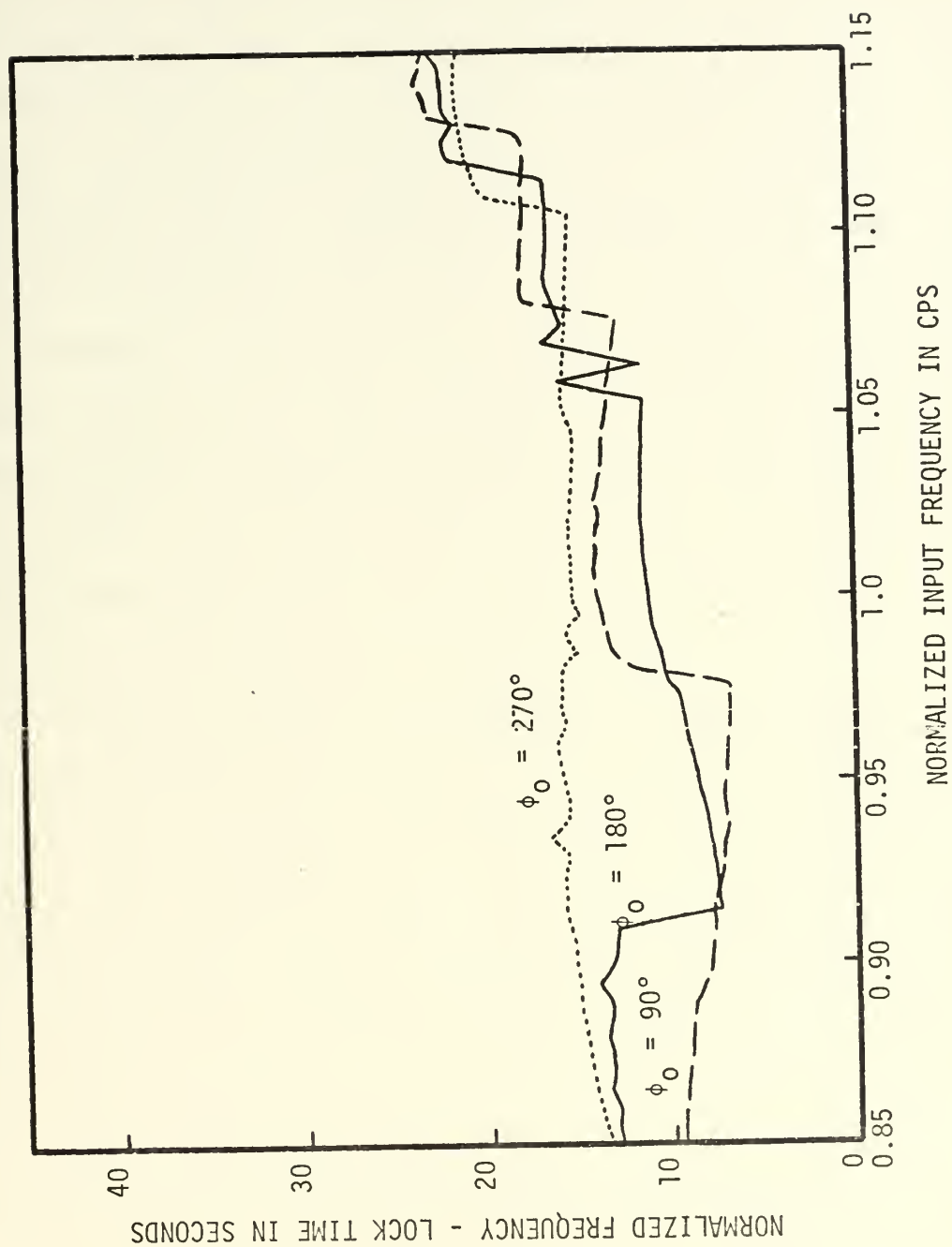


Figure V-B-8. Normalized Frequency-Lock Time as a Function of Normalized Input Frequency for the R-S Nonlinear Phase Comparator with a Gain of 0.002, TC of 5.0, and for Various Values of Initial Phase.

comparator and the nonlinear phase comparator becomes more pronounced as the initial phase angle deviates further from its steady state value. This correlates with the information obtained from Figure V-B-7, where it was seen that there existed very little diversity in lock time as the phase was varied across the entire range, while for the normal R-S phase comparator the lock time significantly increased for phase angles which deviated from the steady state value. Therefore, when the curve for $\phi_0 = 90$ degrees in Figure V-B-8 was replaced by another curve for $\phi_0 = 30$ degrees, there was very little difference; while, when this same substitution was made in Figure IV-B-1 for the normal R-S phase comparator, there resulted a large jump in lock times. This is in concurrence with what had been stated earlier about the nonlinear phase comparator yielding a relatively flat response as a function of phase.

The effects of changing the system gain are shown in Figure V-B-9 where the normalized time of phase-lock is plotted as a function of normalized input frequency for an initial phase of 180 degrees and for various values of the system gain. The curves of Figure V-B-9 can then be compared with the curves for corresponding values of gain but using the normal R-S phase comparator as shown in Figure IV-C-4. Starting with a value of gain = 0.001, it is seen that the curves for the normal and nonlinear phase comparators demonstrate approximately equal phase-lock times until the input frequency variation becomes greater than ± 10 percent of the VCO frequency; at which point the R-S nonlinear circuit begins to demonstrate vastly superior performance. For intermediate values of gain such as 0.002 and 0.004, the R-S nonlinear phase comparator is again superior for high values of input frequency, but for some low values of input frequency the phase-lock time for the nonlinear circuit is greater than that of the linear circuit. For large values of gain such as 0.008

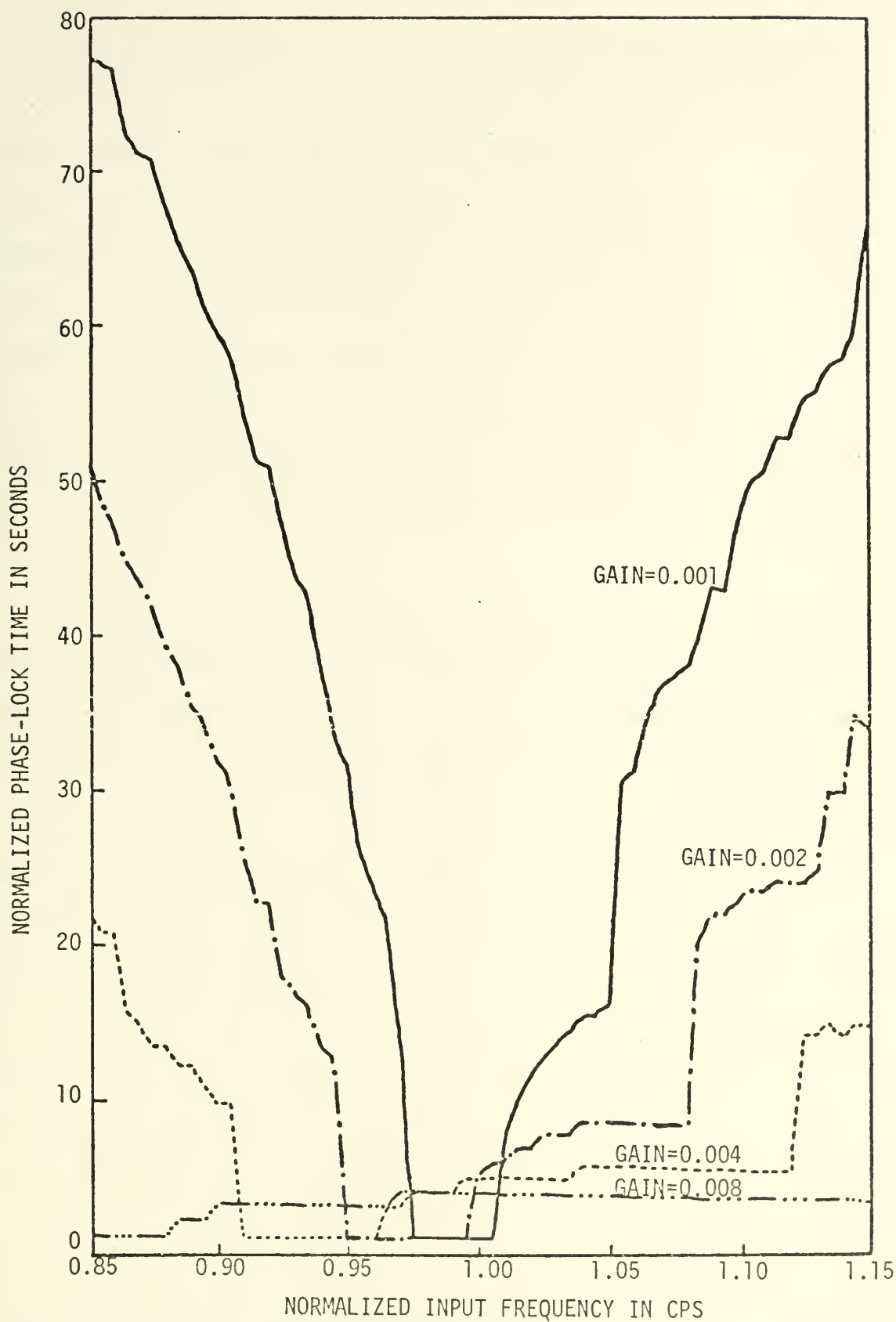


Figure V-B-9. Normalized Phase-Lock Time as a Function of Normalized Input Frequency for the R-S Nonlinear Phase Comparator with an Initial Phase of 180 Degrees, Time Constant of 5.0, and for Various Values of Gain.

the nonlinear phase comparator has an essentially uniform lock time of only a few seconds over the entire range of frequencies considered, and is again superior to the normal R-S phase comparator.

The curves of Figure V-B-9 conform to theory except for the region of intermediate gain at low input frequencies. Here the phase-lock times appeared to be greater than anticipated, and further research was required to explain this phenomenon. Investigation revealed that for initial phase angles other than those in the vicinity of the steady state value, the phenomenon discussed above did not exist, and the nonlinear circuit produced lock quicker than the linear circuit for essentially all values of gain.

To explain the circuit performance it is necessary to understand the complex relationships which exist between the phase comparator gain, the input phase, and the period of the input signal. Up to this point all previous discussion of circuit performance has assumed that the phase comparator gain $\frac{df(\phi_{on})}{d\phi_{on}}$ was constant for all values of input frequency. However, a closer investigation has shown this assumption to be only an approximation. In the nonlinear phase comparator the instantaneous output of the phase comparator is not a constant, but is a function of time. It is then necessary to go back to Equation V-b-1 where the phase comparator output was expressed as a difference between integrals whose limits were given in terms of the normalized phase, and realize that this equation only holds for the condition where the normalized input frequency is unity and therefore the time required for the input waveform to vary through 360 degrees of its phase is one second. If the normalized input frequency were different from unity then Equation V-b-1 must be rewritten as

$$f(\phi_{on}) = \int_0^{t_1} \text{AMP} e^{-TC t} dt - \int_0^{PD-t_1} \text{AMP} e^{-TC t} dt, \quad (\text{V-b-6})$$

where PD is the period of the normalized input frequency and t_1 is the normalized time corresponding to the phase difference between the input and VCO pulses. The parameter t_1 may be expressed as

$$t_1 = \phi_{on} PD. \quad (\text{V-b-7})$$

The gain characteristic of the phase comparator can then be expressed in terms of TC, ϕ_{on} , and PD, and given as

$$\frac{df(\phi_{on})}{d\phi_{on}} = \text{AMP} \left[e^{-TC \phi_{on} PD} + e^{-TC(PD - \phi_{on} PD)} \right]. \quad (\text{V-b-8})$$

The earlier gain equation (Equation V-b-3) and the family of curves shown in Figure V-B-2 are good only for the condition where the normalized input frequency is 1.0 cps, and these curves must be modified before they can be applied exactly for any other input frequency. The additional perturbations on the nonlinear phase comparator characteristic curves caused by variations of the input frequency were computed using a digital program and the results are provided by Figure V-B-10 for the condition of TC = 5.0 and for values of ϕ_{on} in 0.1 unit steps. The values of gain shown in Figure V-B-10 for a normalized input frequency of 1.0 concur exactly with the values shown in Figure V-B-2, and the remaining portions of the curve demonstrate how the gain changes with variations of the input frequency. The curves of Figure V-B-10 show a significant difference in the effect of frequency for different values of ϕ_{on} . For ϕ_{on} near the steady state value the phase comparator gain increases with increasing frequency. However, for the normalized input phase near either its high or low extremes the effect is just the opposite, and here

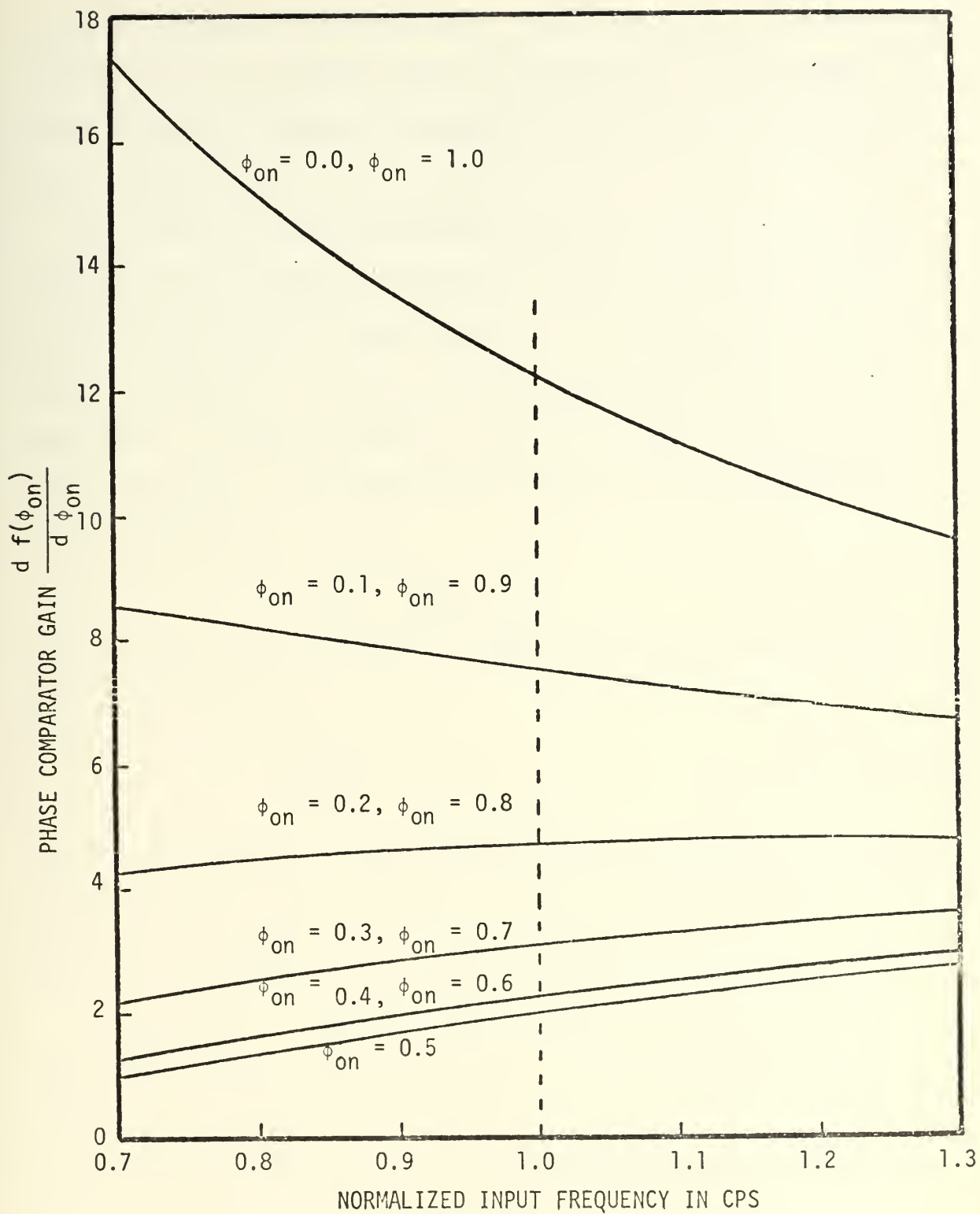


Figure V-B-10. Phase Comparator Gain for the R-S Nonlinear Phase Comparator as a Function of the Normalized Input Frequency for TC of 5.0 and ϕ_{on} in 0.1 Steps.

the gain decreases with an increase in input frequency. Since the phase comparator gain is cascaded with all the other gains of the system, the entire loop gain increases or decreases linearly with the change of the phase comparator gain.

The variation of phase comparator gain with changes in the input frequency is not limited to the nonlinear phase comparator, but also exists in the normal R-S phase comparator where the variation takes on a quite different form. If the average output of the normal R-S phase comparator is computed considering the effects of the input frequency and employing the same notation used in Equation V-b-6, then the output can be expressed by

$$f(\phi_{on}) = PD(2 \phi_{on} - 1) \quad . \quad (V-b-9)$$

From Equation V-b-9 it is easy to compute the normal R-S phase comparator gain as

$$\frac{df(\phi_{on})}{d \phi_{on}} = 2 PD \quad . \quad (V-b-10)$$

Equation V-b-10 shows that the normal R-S phase comparator gain remains a constant for all values of phase, but that the gain decreases in inverse proportion to increases in the input frequency.

With the help of Equations V-b-9 and V-b-10 together with Figure V-B-10 it is now possible to explain the apparent abnormalities of Figures V-B-9 and IV-C-4. The phase angle for the curves in Figure V-B-9 was 180 degrees, and a check of Figure V-B-10 shows that for $\phi_{on} = 0.5$ the phase comparator gain decreases with decreasing frequency. This explains why it took a longer time for the system to lock for input frequencies a fixed amount below the center frequency than for input frequencies the same fixed amount above the center frequency, as was

observed in the curves of lock time versus frequency for the nonlinear phase comparator. The reason why the lock times for low frequencies were observed to increase for $\phi_0 = 180$ degrees but not for large or small values of ϕ_0 is also evident from the curves of Figures V-B-10, where it is seen that for large or small values of ϕ_0 the system gain increases as input frequency decreases. In addition, Equation V-b-10 explains why the lock times for the normal R-S phase comparator are greater for the high frequencies than for the low frequencies as seen in Figure IV-C-4. With this new knowledge of how the phase comparator characteristics respond to variations of the input frequency, together with the understanding of how the gain varies with the input phase angle, a complete interpretation of the curves of phase-lock versus frequency is now possible.

The above investigation of the phase comparator's gain variation as a function of input frequency has not been previously accomplished for any phase comparator. Nevertheless, it is believed to be an important achievement towards helping to understand the complete circuit operation by thoroughly analyzing the characteristics of each component part. By being able to isolate the phase comparator characteristics from the rest of the circuit and by being able to accurately describe these characteristics with equations and graphs, it has been possible to explain certain overall circuit performance characteristics which could not otherwise be explained. In addition, since it is now possible to make a correlation between performance characteristics and specific circuit components, a powerful tool has been added to aid in the design of desired characteristics into specific phase-locked loop circuits. This analysis of the gain characteristics of the phase comparators as a function of frequency

also provides another norm to be used when comparing different types of phase comparators.

Data was also taken to show the variation of the seize frequency as a function of phase for the nonlinear phase comparator. In Figure V-B-11 the loop gain was held fixed at 0.002, and curves were obtained for increasing magnitudes of the time constant for both high and low values of seize frequency. It was seen that as the time constant increased, the seize frequency also increased in a uniform manner until the time constant became so large that the circuit operation tended to behave erratically. A comparison can easily be made between Figure V-B-11 and the curves for the normal R-S phase shown in Figure IV-E-3, since the curve for the nonlinear phase comparator with a time constant of 1.0 is just slightly greater than that of the normal R-S phase comparator with a gain of 0.002. All other curves of Figure V-B-11 show a significantly larger value of seize frequency than that for the normal R-S phase comparator for the same value of gain.

A second family of curves was prepared to show the variation of seize frequency as a function of gain with the time constant held fixed at 5.0. These curves are shown in Figure V-B-12, and again demonstrate a wider range of seize frequency for a given value of gain than was available using the normal R-S phase comparator. In both Figures V-B-11 and V-B-12 the curves tend to become erratic as either the gain or time constant is increased beyond appropriate limits. This spasmodic reaction of the seize frequency curves to increased gain is also seen to occur in Figure IV-E-3 for the normal R-S phase comparator. Although the lock times may tend to vary widely for only minor changes in the input conditions when operating under high gain, it should be noted that the system with either

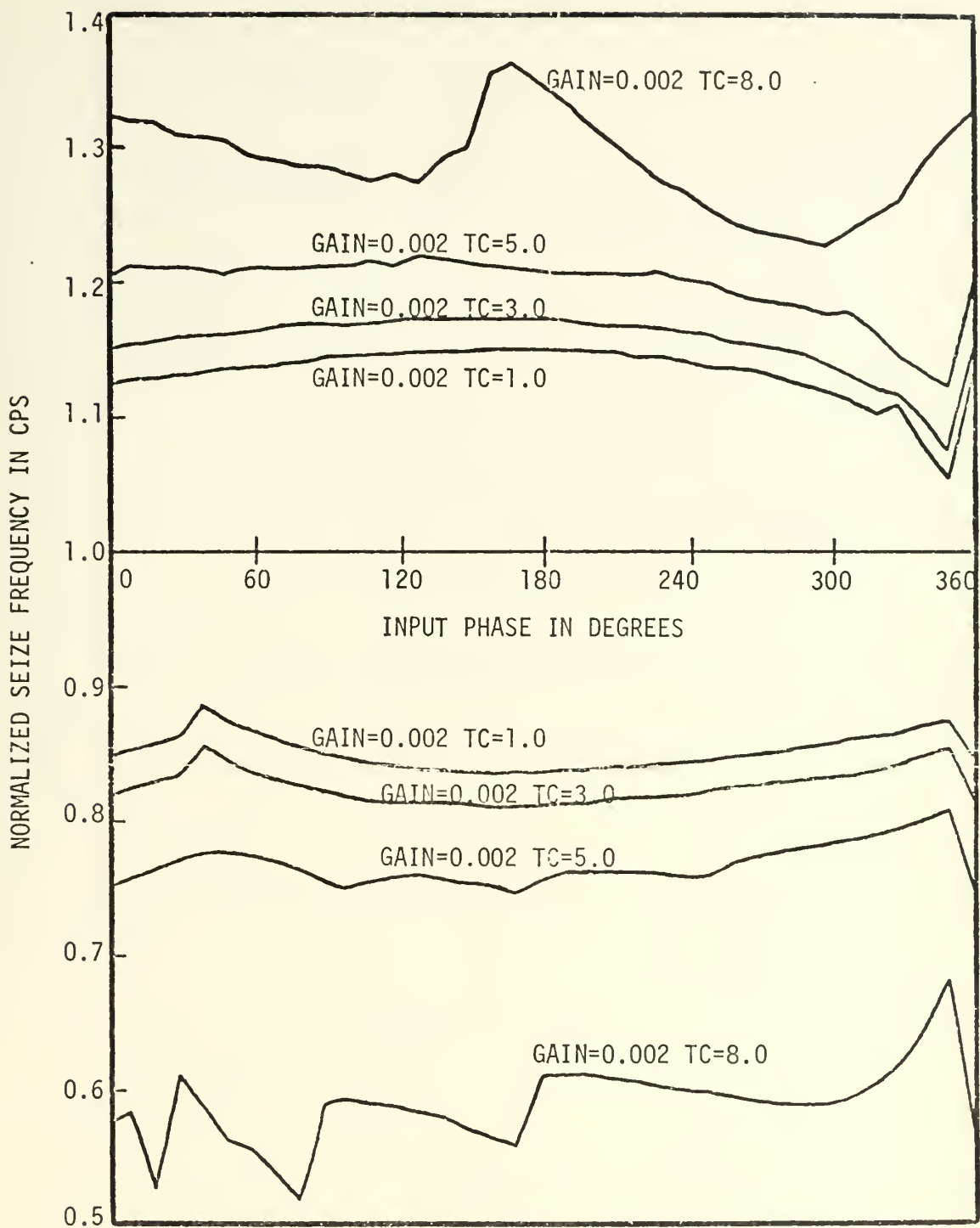


Figure V-B-11. Normalized Seize Frequency as a Function of Initial Phase for the R-S Nonlinear Phase Comparator with a Gain of 0.002 and for Various Values of TC.

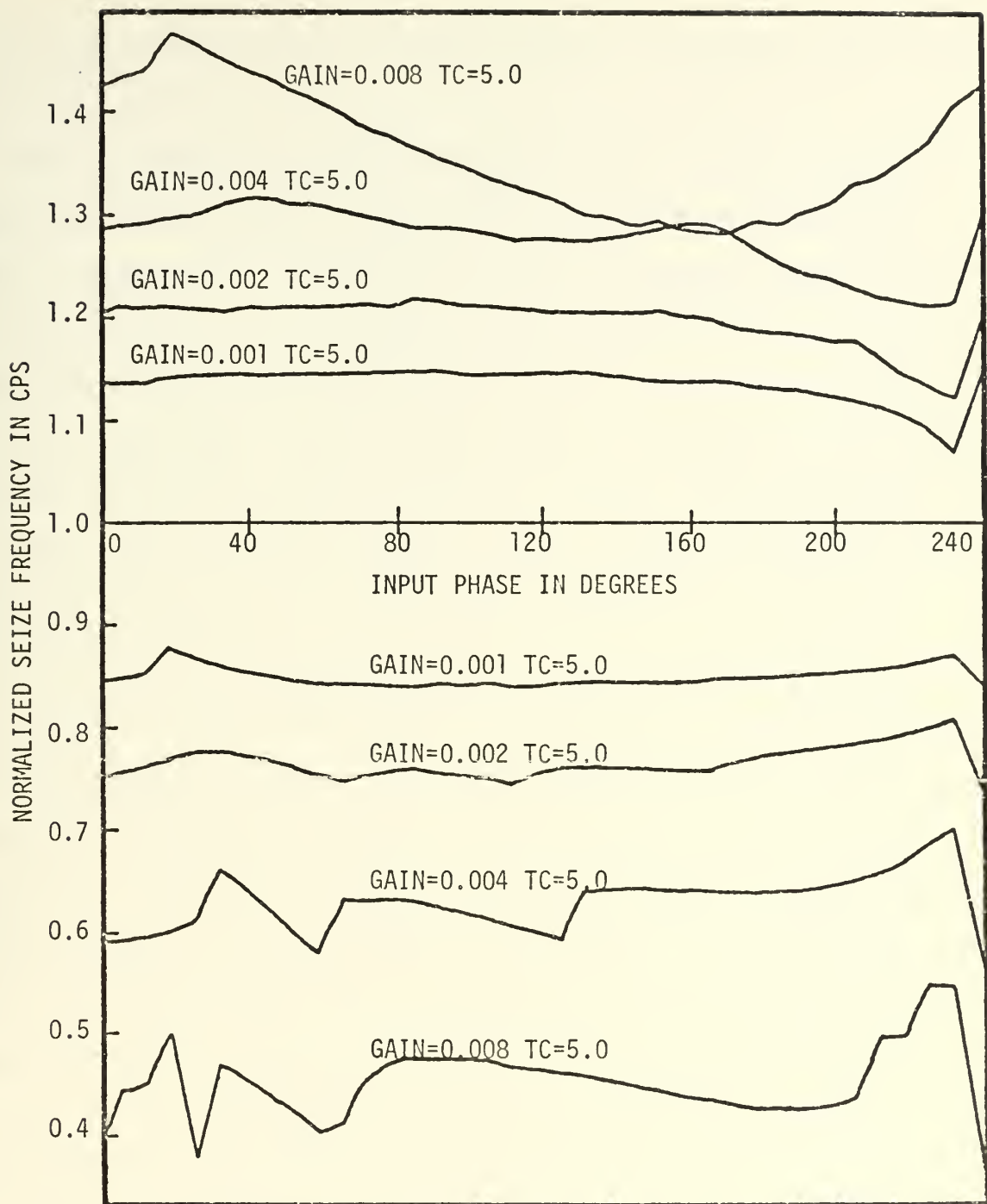


Figure V-B-12. Normalized Seize Frequency as a Function of Initial Phase for the R-S Nonlinear Phase Comparator with a Time Constant of 5.0 and Various Values of the Loop Gain.

the normal or the nonlinear R-S phase comparator did remain stable for all values of gain.

The instantaneous frequency variation of the R-S nonlinear phase comparator is very similar to that of the normal R-S phase comparator shown in Figure V-A-1, except that now the instantaneous variation has actually increased. This increase is due to the fact that during each cycle of the input waveform the phase comparator output is now switched to $\pm \text{AMP}$, where AMP is usually greater than the 1.0 which is used as the switched value for the normal R-S phase comparator. The instantaneous frequency variation for the nonlinear phase comparator with a gain of 0.002 and time constant of 5.0 is shown in Figure V-B-13, where one curve is a plot of the average normalized frequency error as a function of time and the second curve shows the instantaneous normalized frequency error as a function of time. Here, as in Figure V-A-1, it is seen that even under steady state conditions the instantaneous frequency error varies over wide limits, and these variations increase in amplitude as either the gain or the time constant is increased. For large values of gain or for large values of the time constant, this instantaneous frequency variation can become so large that it causes the VCO to vary throughout its entire range of operation allowed by the circuit configuration.

The performance of the R-S nonlinear phase comparator under zero-input conditions is quite different from that of the normal R-S phase comparator. In the absence of an input signal the nonlinear phase comparator flip-flop also remains in a reset condition indefinitely, but now the phase comparator does not continuously provide a constant amplitude output. Instead, its output is reduced exponentially to zero with the

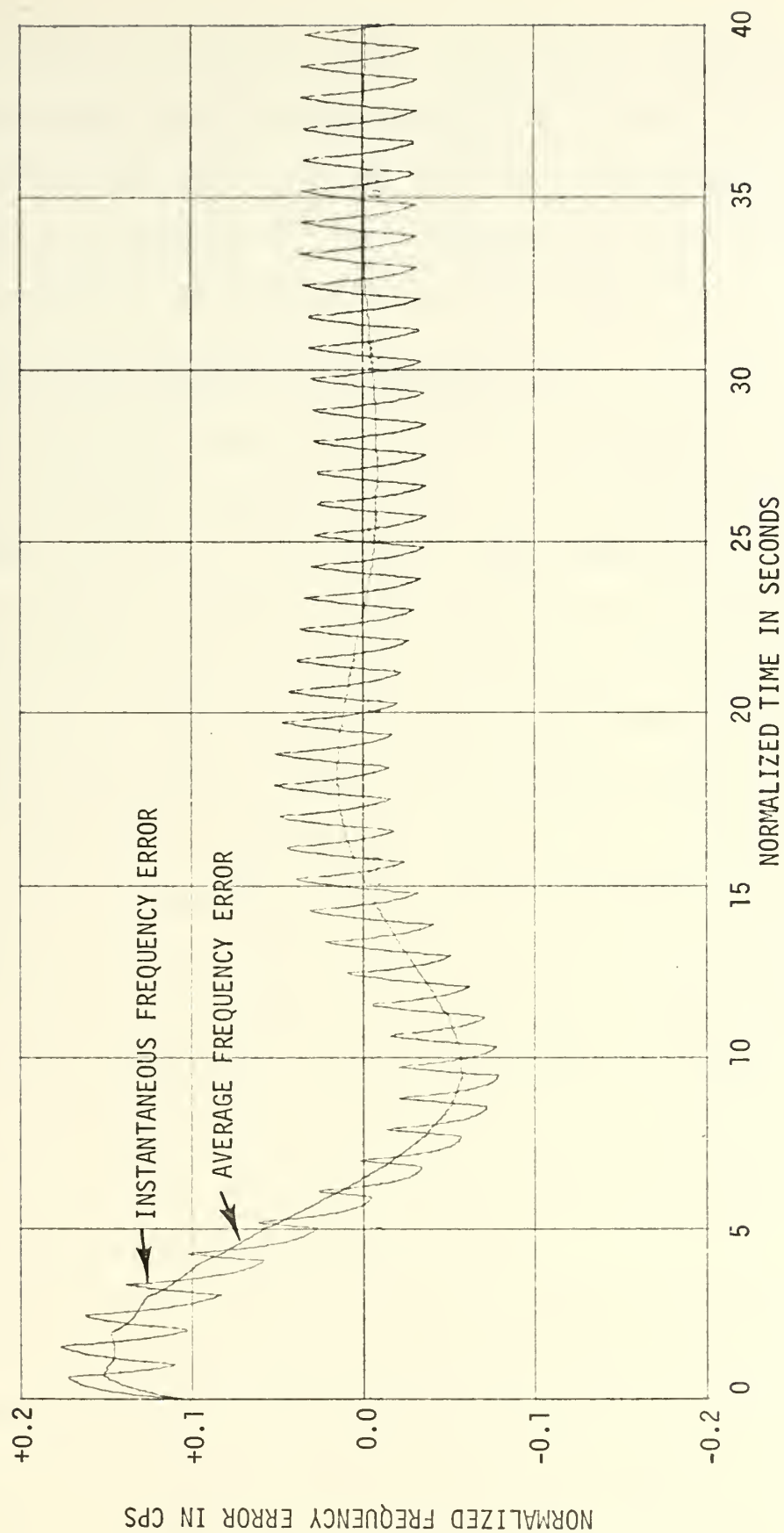


Figure V-B-13. Instantaneous and Average Normalized Frequency Error as a Function of Normalized Time for the R-S Nonlinear Phase Comparator with a Gain of 0.002, TC of 3.0, f_{in} of 1.1 cps, and ϕ_0 of 90 Degrees.

time constant TC , and will remain at zero thereby allowing the VCO to continue operating at a frequency only slightly lower than its frequency at the time the input signal was lost. Thus the nonlinear phase comparator has attained a much greater degree of stability under zero-input conditions than the normal R-S phase comparator.

C. R-S PHASE COMPARATOR WITH TRACK AND HOLD

A circuit modification will now be discussed which is not an alteration to the phase comparator directly, but is closely connected to the concepts discussed in this section on phase comparators. This modification consisted of inserting a track and hold circuit between the filter output and the input to the VCO. The track and hold circuit was designed to sample the filter output at the occurrence of each pulse from the VCO, and hold the control voltage to the VCO constant at the sampled value until the arrival of another pulse from the VCO. The motivation for adding the track and hold circuit arose from a desire to further investigate the sample data concepts discussed previously in Subsection IV, G and to see the effects of a true sampling system on the phase-locked loop performance. A second objective was to develop a circuit where the instantaneous frequency variation of the VCO in steady state operation would approach zero. In the following paragraphs it will be seen how these objectives were fulfilled.

In the analog simulation the circuit modification consisted of simply inserting a standard track and hold circuit which was available as a patchable component on the CI-5000 computer. This track and hold circuit consisted of a high gain amplifier and a relay connected as shown in Figure V-C-1. In the track position the circuit functions as a unity gain amplifier with the output voltage following or tracking the input

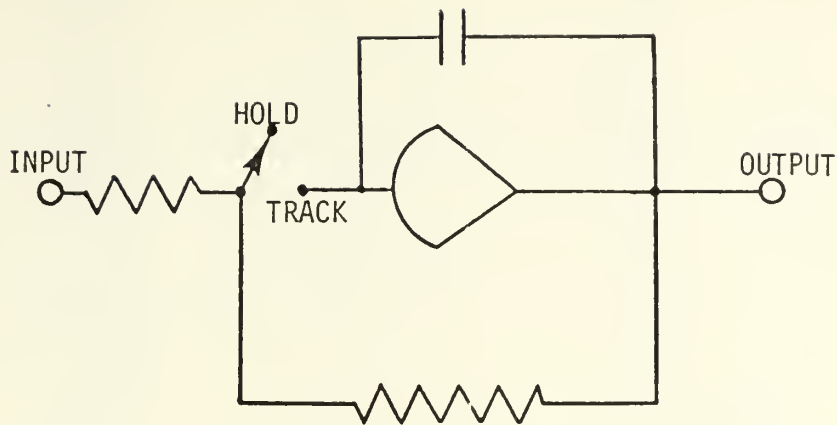


Figure V-C-1. Analog Track and Hold Circuit

voltage, and in the hold position the capacitor holds the output voltage fixed at the last value it had when the relay was switched to the hold position. The track and hold circuit was connected so that it would track only for the duration of the VCO pulse, and would then hold its value until the arrival of the next VCO pulse. The digital simulation was similarly altered using logic statements to make the VCO frequency correspond to the filter output at each occurrence of a VCO pulse, and then retain the VCO frequency at that value until the next VCO pulse. The operation of the system using the R-S phase comparator with track and hold is shown in Figure V-C-2, which was obtained using the digital simulation with normalized input frequency of 1.1 cps and an input phase of 90 degrees. Part (a) of Figure V-C-2 contains two curves, one of which is the sawtooth variation in output frequency due to the normal output of the R-S phase comparator, and the second curve consists of the step function output of the track and hold circuit, which corresponds to the value of the R-S output only at the time of each VCO pulse. Part (b) of Figure V-C-2 was made under exactly the same operating conditions as

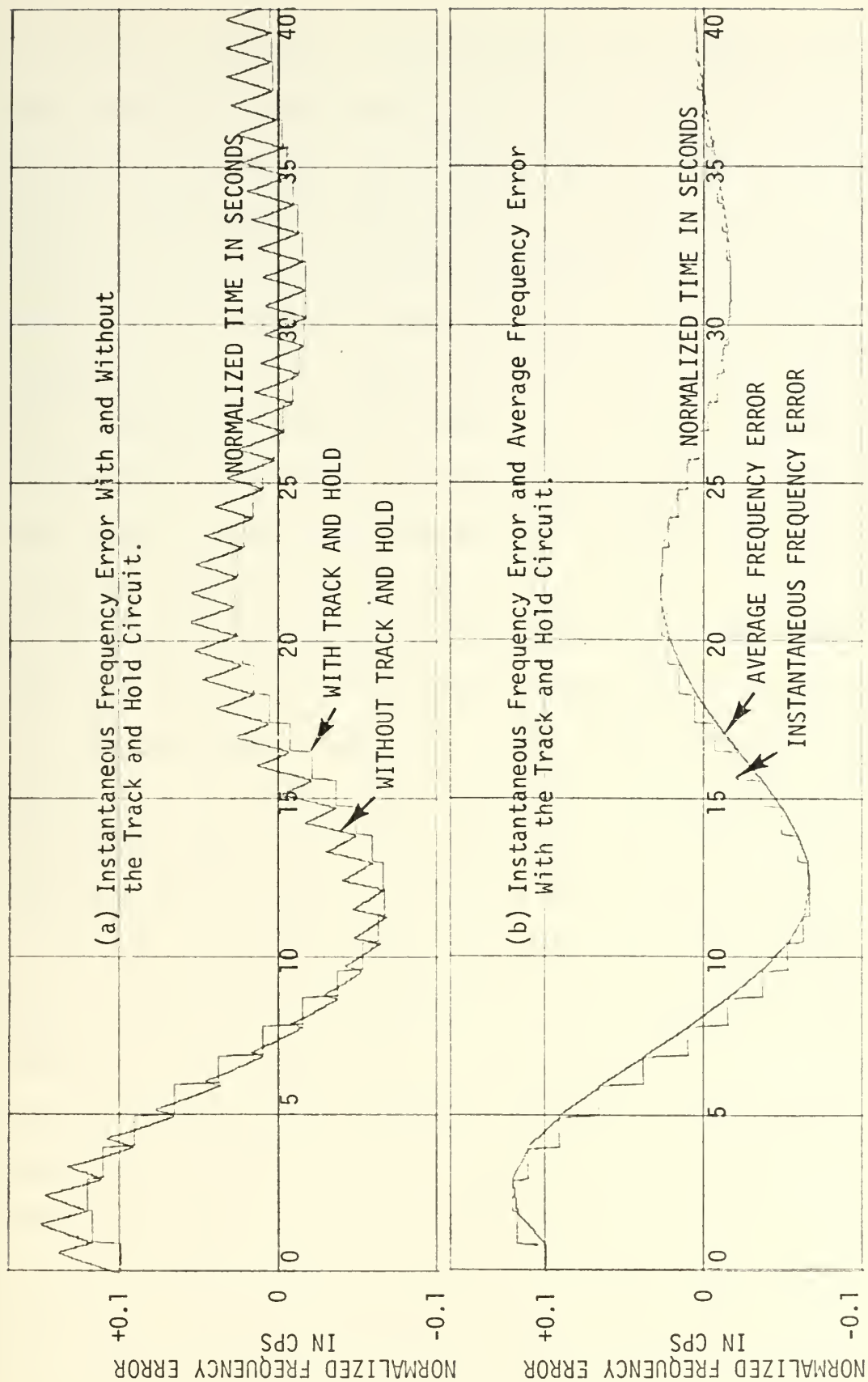


Figure V-C-2. Plots of Frequency Error Versus Normalized Time to Demonstrate the Operation of the R-S Phase Comparator with Track and Hold.

in part (a), and therefore the step output of the track and hold network is identical in both part (a) and part (b). The difference between the two parts of Figure V-C-2 is that the second curve in part (b) shows how the average frequency error varies as a function of time. It is now possible to discuss one of the advantages of the R-S track and hold circuit, which is that for steady state operation both the average VCO frequency error and the instantaneous VCO frequency error approach zero, as is portrayed in part (b) of Figure V-C-2. This is consistent with the results obtained previously for the R-S phase comparator shown in Figure V-A-1 where the steady state instantaneous frequency error was seen to have a zero mean and a constant amplitude variation, so that any sampling of its waveform at a sampling period corresponding to an integral number times the period of the instantaneous frequency variation would result in a constant output. Therefore, in the R-S track and hold circuit under steady state operation the VCO does not sweep through a wide range of frequency during each period of the input signal, and this might be of considerable advantage in particular circuit applications.

The average normalized frequency error as a function of normalized time for the R-S phase comparator with track and hold is plotted in Figure V-C-3 for several values of the circuit gain. It is immediately obvious that the system response for the track and hold circuit varies markedly from that of either the normal R-S or R-S nonlinear circuit, in that instability is reached with the track and hold circuit for a relatively low value of gain. In fact, the curves of Figure V-C-3 correlate quite well with the data plotted in Figure IV-G-1 which shows the open-loop Bode diagram for the system with the addition of a sample and hold circuit in series. Figure V-C-3 shows that the limit of stability is reached for a gain of about 0.008, and that for gains higher than 0.008

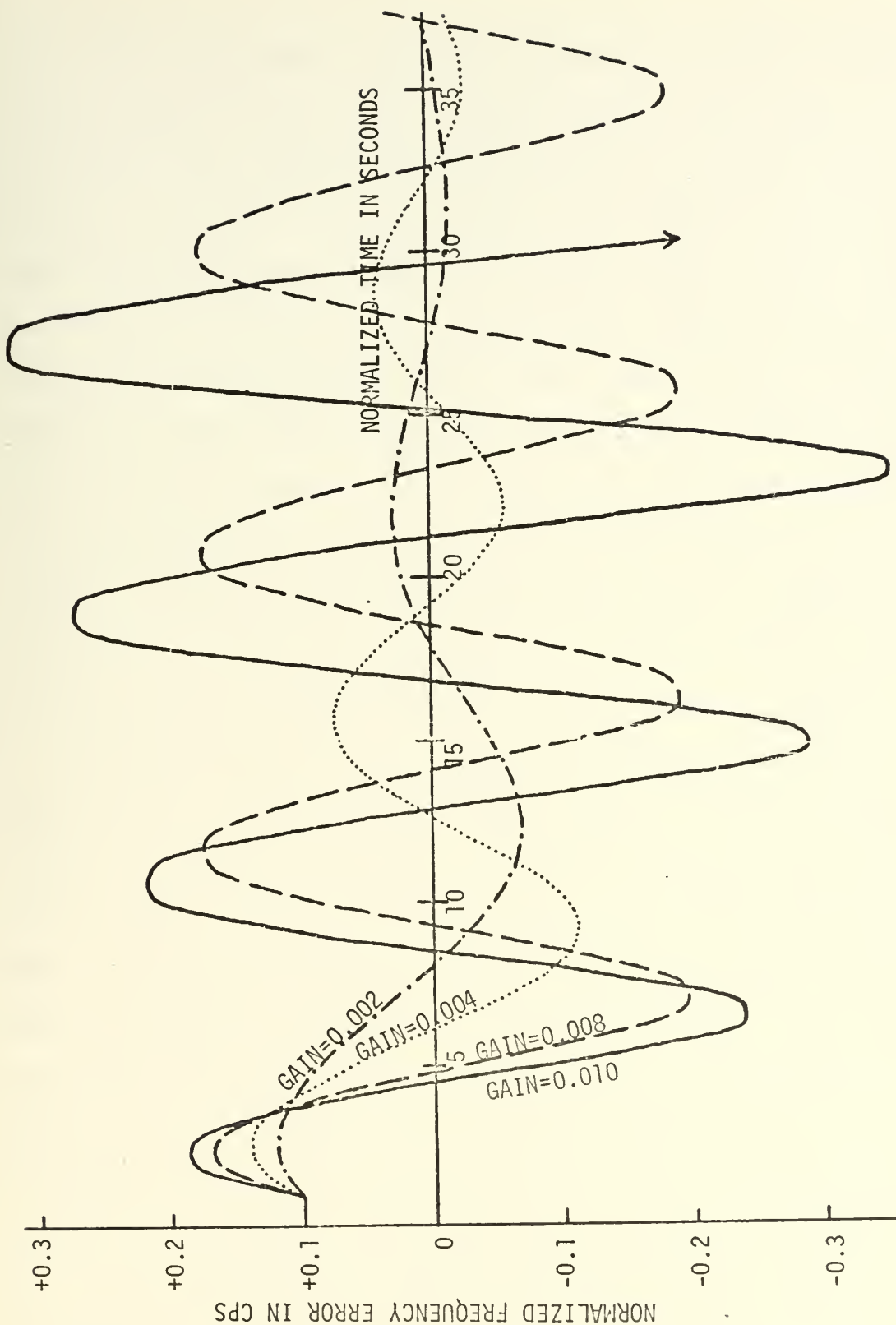


Figure V-C-3. Normalized Frequency Error as a Function of Normalized Time for the R-S Phase Comparator with Track and Hold for an Input Frequency of 1.1 cps and ϕ_0 of 90 degrees.

the system output grows in magnitude and results in complete instability. The Bode plot of Figure IV-G-1 indicates that the system should already be unstable for a normalized sampling rate of 1.0 cps and a gain of 0.008, but there are several correction factors which must first be applied before this Bode diagram is entirely accurate. One correction factor would be to draw in the actual magnitude curve instead of using the straight line approximation, and this would lower the gain curve by several db in the region of the gain-crossover point. Another correction that could be applied would be to adjust the magnitude curve for the sampling effects of the track and hold circuit, but as pointed out earlier, this would lower the magnitude curve by only an amount of less than one db. A third factor would be to consider the sampling effect of the R-S phase comparator which is in cascade with the sampling effect of the track and hold circuit, although this effect has been shown in Subsection IV, G to be relatively small. The last factor to consider is that for the curves of Figure V-C-3 the input frequency was 1.1 cps, and therefore, since the VCO frequency varies about this steady state value and because the sample rate equals the VCO frequency, the average sampling frequency was actually 1.1 cps and not 1.0 cps. It is difficult to estimate the effect of this variation of the sampling rate with changes in the VCO frequency, since the VCO frequency varies over a relatively wide range as seen from Figure V-C-3. If all the correction factors described above were applied to the Bode plot of Figure IV-G-1 for a sample frequency of 1.0 cps, the limiting gain for stable operation should appear at about 0.008 and thus concur with the actual simulation results.

In order to study the system performance as a function of initial phase, the family of curves shown in Figure V-C-4 was computed using

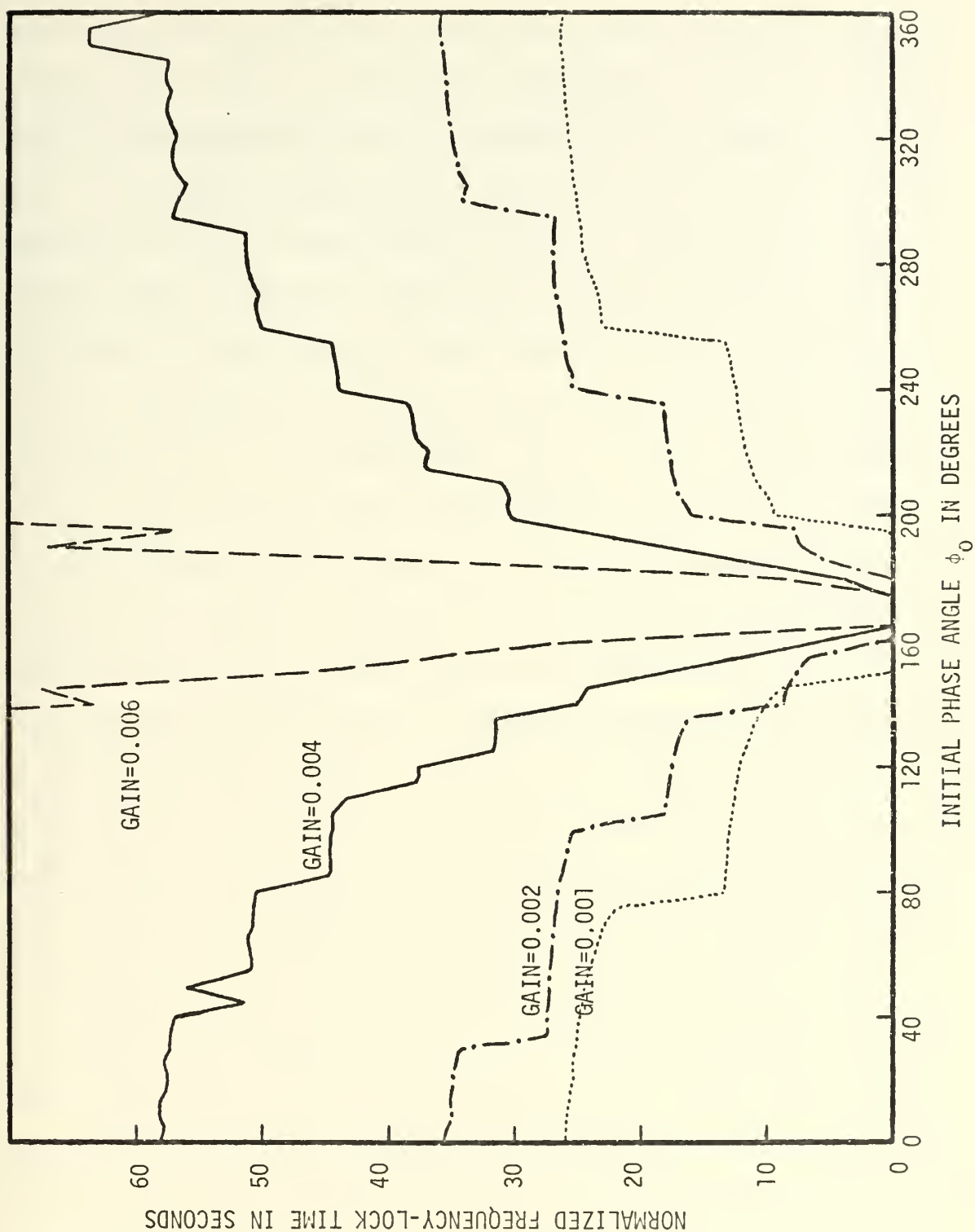


Figure V-C-4. Frequency-Lock Time as a Function of Input Phase for the R-S Phase Comparator with Track and Hold Operating with a Normalized Input Frequency of 1.0 cps and Various Values of Gain.

the digital simulation and was provided to show the variation of the frequency-lock times as a function of initial phase angle for various values of the system gain and for a normalized input frequency of 1.0 cps. The contrast between the R-S track and hold circuit and the R-S nonlinear circuit is readily obvious since the track and hold curves exhibit a wide variation of lock time as a function of phase for any fixed value of gain, while for the R-S nonlinear phase comparator the curves of frequency-lock time versus phase shown in Figure V-B-7 are relatively flat. The frequency-lock times for the R-S track and hold circuit are also greater than either those for the normal R-S or for the R-S nonlinear circuit, except for a very narrow region around the value of the steady state phase. Perhaps the most obvious difference between the curves of frequency-lock time versus phase for the R-S track and hold circuit and the corresponding curves for the normal R-S or the R-S nonlinear circuit is the fact that for the R-S track and hold circuit the lock time increases with increasing gain, while for the other systems studied so far the lock times decreased for an increase in gain. The reason why the lock times of Figure V-C-4 increased with gain was because of the diminished stability of the circuit due to the reduction of the phase margin as a result of the sampling effects of the track and hold circuit as shown in Figure IV-G-1. Due to the increased oscillatory nature of the system with the track and hold circuit present, it took longer for the system to steady out and attain lock than for the previous systems which were more highly damped.

Experimental data was taken to investigate the circuit performance as a function of input frequency, and Figure V-C-5 shows the normalized frequency-lock time as a function of normalized input frequency for three

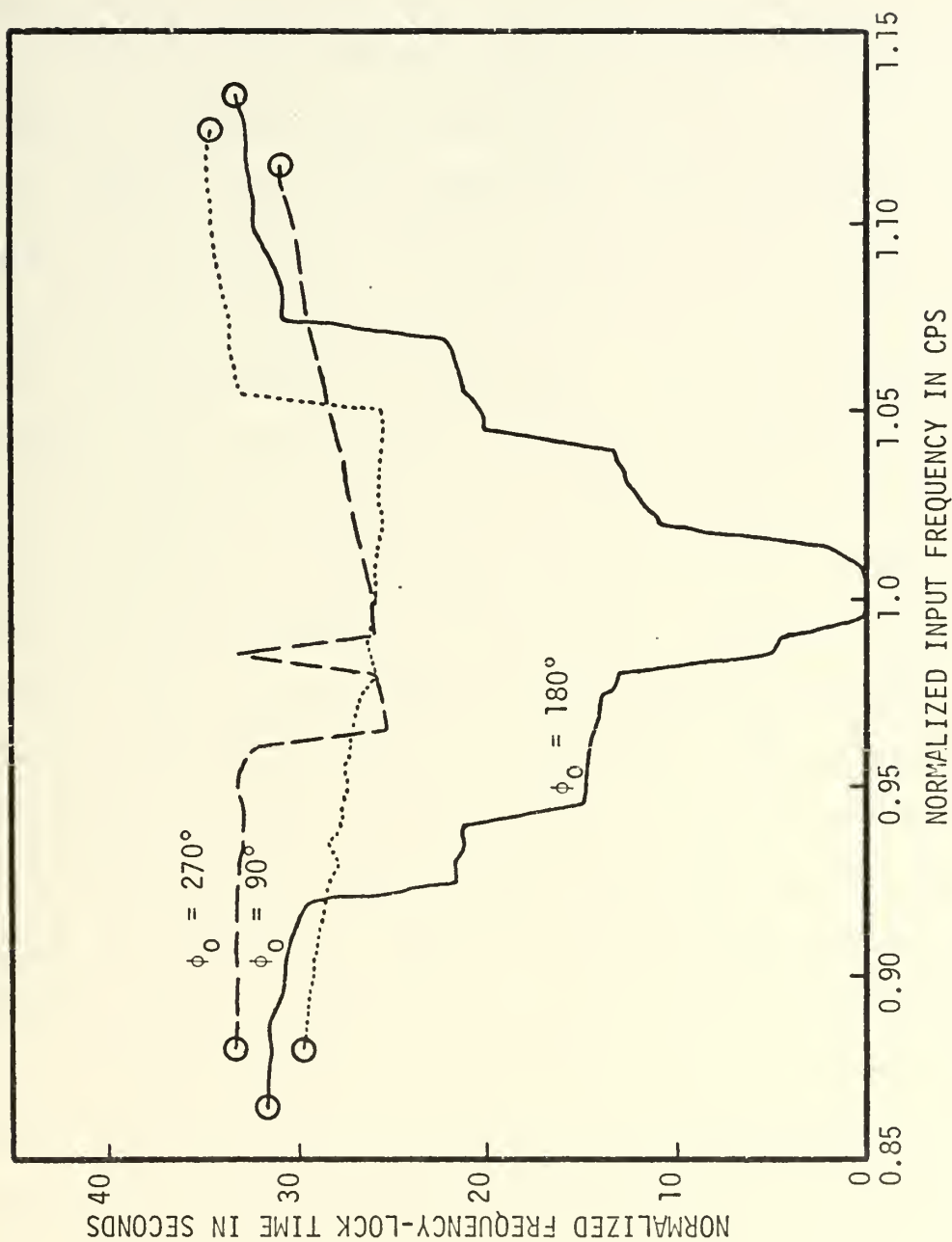


Figure V-C-5. Frequency-Lock Time as a Function of Input Frequency for the R-S Phase Comparator with Track and Hold for a Gain of 0.002 and for Various Values of Initial Phase.

values of input phase. The circled points at the end of each curve denote the fact that these were the limiting frequencies for which lock had occurred, and this failure to lock introduced a new phenomenon not previously experienced with either the normal R-S or the R-S nonlinear phase comparator, since with these phase comparators the lock range appeared to be unlimited. Not only was there a limited range of frequencies over which the system would lock, but these limits were seen to be relatively narrow and restrictive. One item of interest which appeared in the printed results of the digital simulation but which was not apparent from Figure V-C-5 was that for the R-S phase comparator with track and hold the limiting frequency for which lock would occur was also the seize frequency for the system. In effect, if the system skipped a cycle it would never lock, even though simulation runs were made for up to 2000 seconds of normalized time. This failure to lock after having skipped only one cycle was contrary to previous results for the normal R-S and R-S nonlinear phase comparators, since when these systems were subjected to large initial frequency differences many cycles might be skipped and the systems were still able to attain lock. The curves of Figure V-C-5 also show how the limits of lock range change for the three different phase angles shown, with the greatest lock range existing for an initial phase of 180 degrees. This variation with phase will be demonstrated more thoroughly later in this subsection when discussing the seize frequency.

Another family of curves which demonstrate the effect of gain on the frequency-lock time is shown in Figure V-C-6. In Figure V-C-6, as in the curves of frequency-lock time versus phase given in Figure V-C-4, it is seen that the lock time increases with increasing gain. It is also

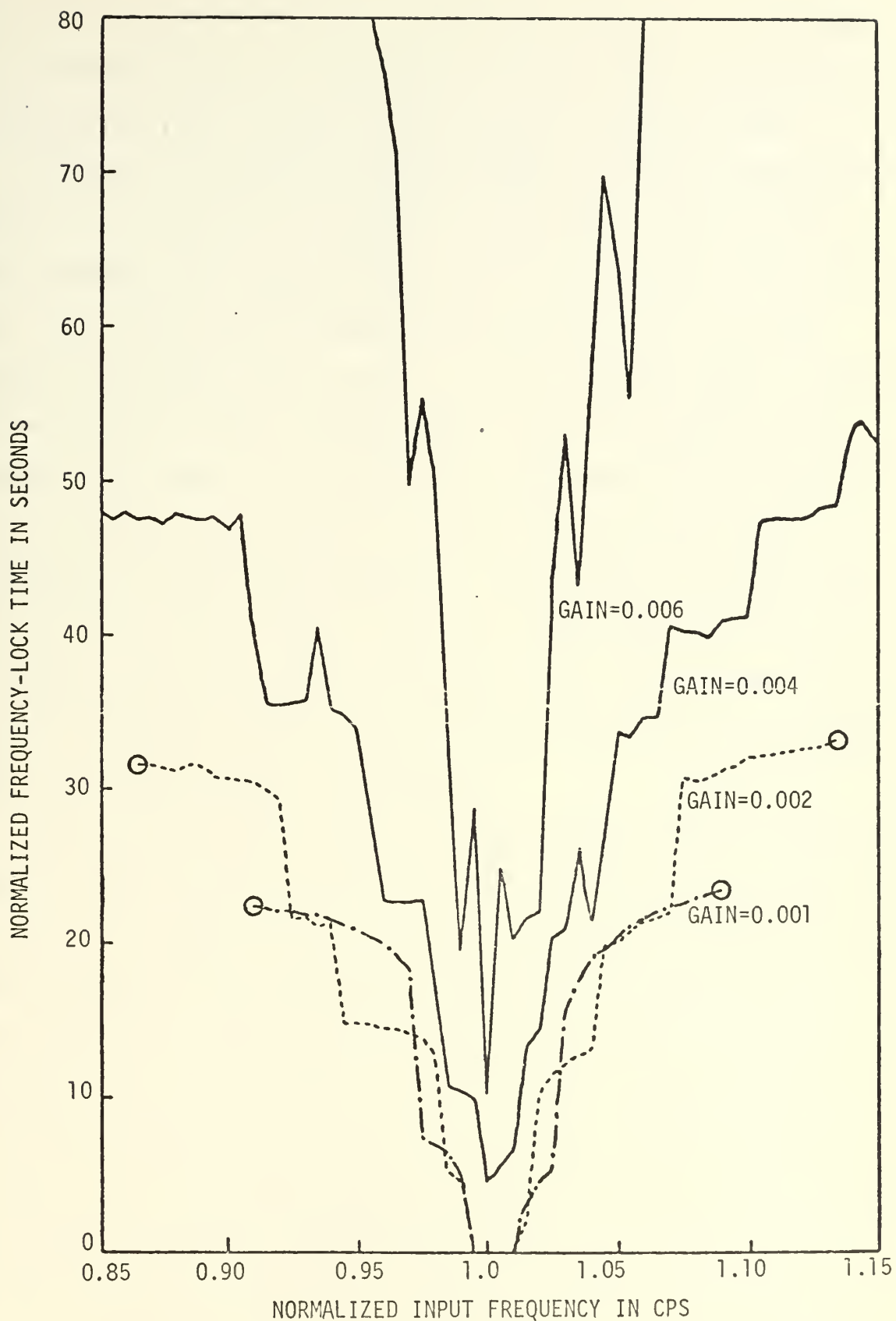


Figure V-C-6. Frequency-Lock Time as a Function of Input Frequency for the R-S Phase Comparator with Track and Hold for an Initial Phase of 180 Degrees and for Various Values of Gain.

observed in Figure V-C-6 that for intermediate values of gain the lock range increases with gain, and although the system will lock for greater frequency deviations, the lock times may become excessively long.

A synopsis of the entire system performance for the R-S phase comparator with track and hold is presented in Figure V-C-7, which shows the seize frequency as a function of phase for various values of the system gain. Due to the particular operating characteristics of the system whereby if the system skips a cycle it fails to lock, the upper and lower seize frequencies shown in Figure V-C-7 are also the upper and lower bounds of the system lock range. The R-S phase comparator with track and hold will always lock over the full range of initial phase for low and intermediate values of gain; however, for high values of gain the system skips cycles and will not lock for initial phases which vary widely from the steady state phase. As the system gain increases, the seize frequency for a high gain is sometimes less than that for a lower value of gain where the system operation is more stable.

In the event the input signal is interrupted, the behavior of the R-S phase comparator with track and hold is similar to the normal R-S circuit in that the filter output is driven to a low negative voltage due to the phase comparator flip-flop being held constantly in a reset condition. The action of the track and hold circuit causes the VCO to track the filter output at the occurrence of each pulse from the VCO, and thus the VCO is also quickly driven to its lowest operating value when the input signal is lost. The above operating condition could be modified by using the input pulse train to control the operation of the track and hold circuit instead of the VCO pulse. If the input pulses were used to control the track and hold circuit, and if for some reason the input pulse train were interrupted; then the control voltage to the VCO would

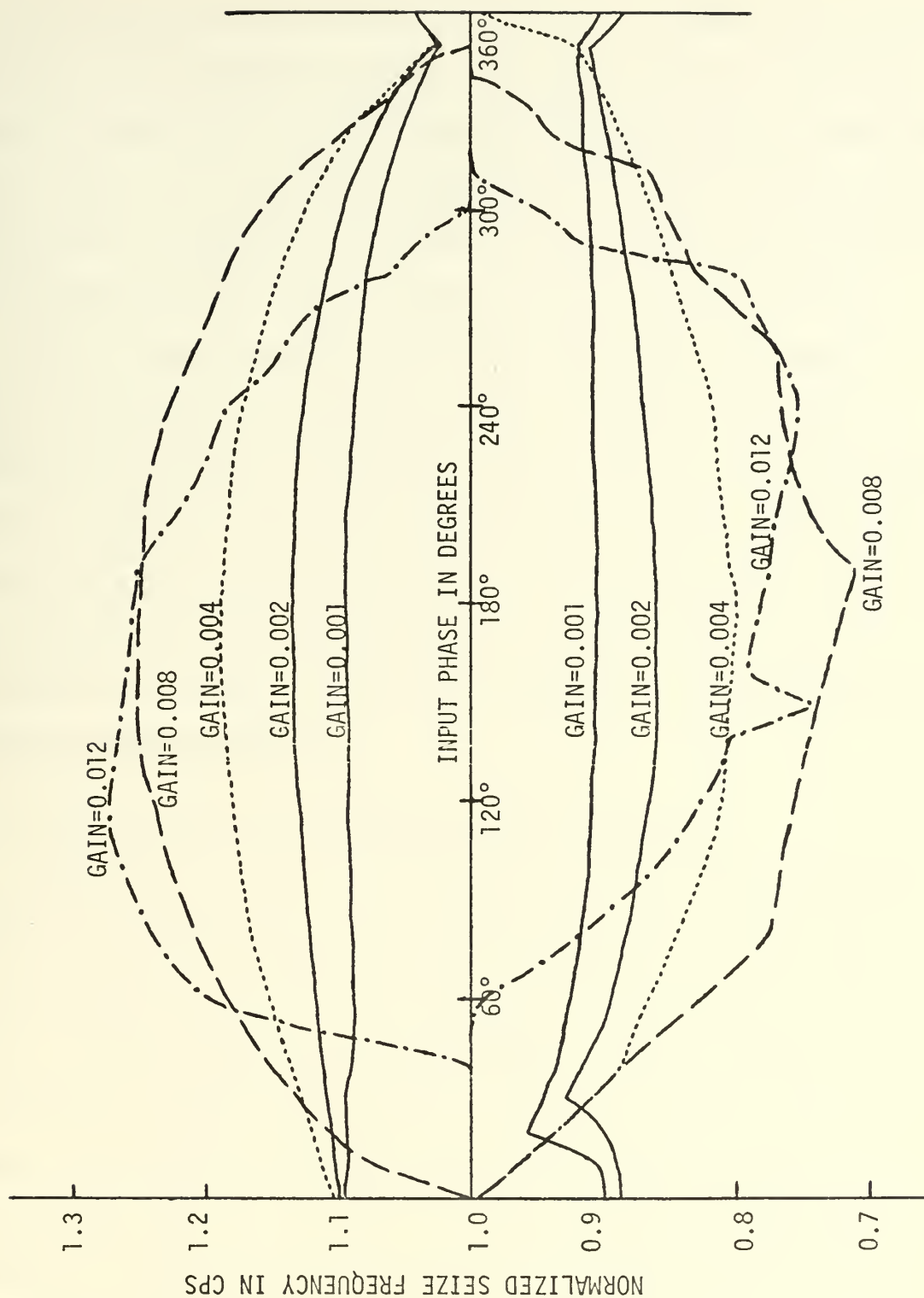


Figure V-C-7. Seize Frequency as a Function of Phase for the R-S Phase Comparator with Track and Hold.

be held constant, and the VCO would continue to operate at the frequency at which it was operating when the input pulse train was interrupted. Thus the circuit can be made to operate effectively with an intermittent input signal, and experimental investigation has shown the other characteristics of its operation to be almost identical when either the input or the VCO pulses are used to control the track and hold circuit.

The R-S phase comparator with track and hold has the advantage of zero instantaneous VCO frequency variation in steady state, and the additional advantage of successful operation with an intermittent input signal. However, it has the disadvantages of a reduced frequency-lock range, and longer frequency-lock times. The track and hold circuit also has the additional disadvantage that an increase in gain results in increased lock times, reduced seize frequency, and ultimately leads to complete system instability.

D. R-S NONLINEAR PHASE COMPARATOR WITH TRACK AND HOLD

An attempt was made to combine the R-S nonlinear phase comparator with a track and hold circuit to obtain the advantages of increased lock range and uniform lock time as a function of phase which are characteristic of the R-S nonlinear phase comparator, together with the zero instantaneous frequency variation and continued operation under zero input conditions which are characteristic of the track and hold circuit. The circuit simulation was carried out using both the analog and digital process by simply combining the nonlinear and the track and hold circuit simulations discussed earlier. The operation of the resultant system is shown in Figure V-D-1 where the average normalized frequency error is plotted as a function of normalized time for an input frequency of 1.1 cps, an initial phase of 90 degrees, a time constant of 5.0, and for

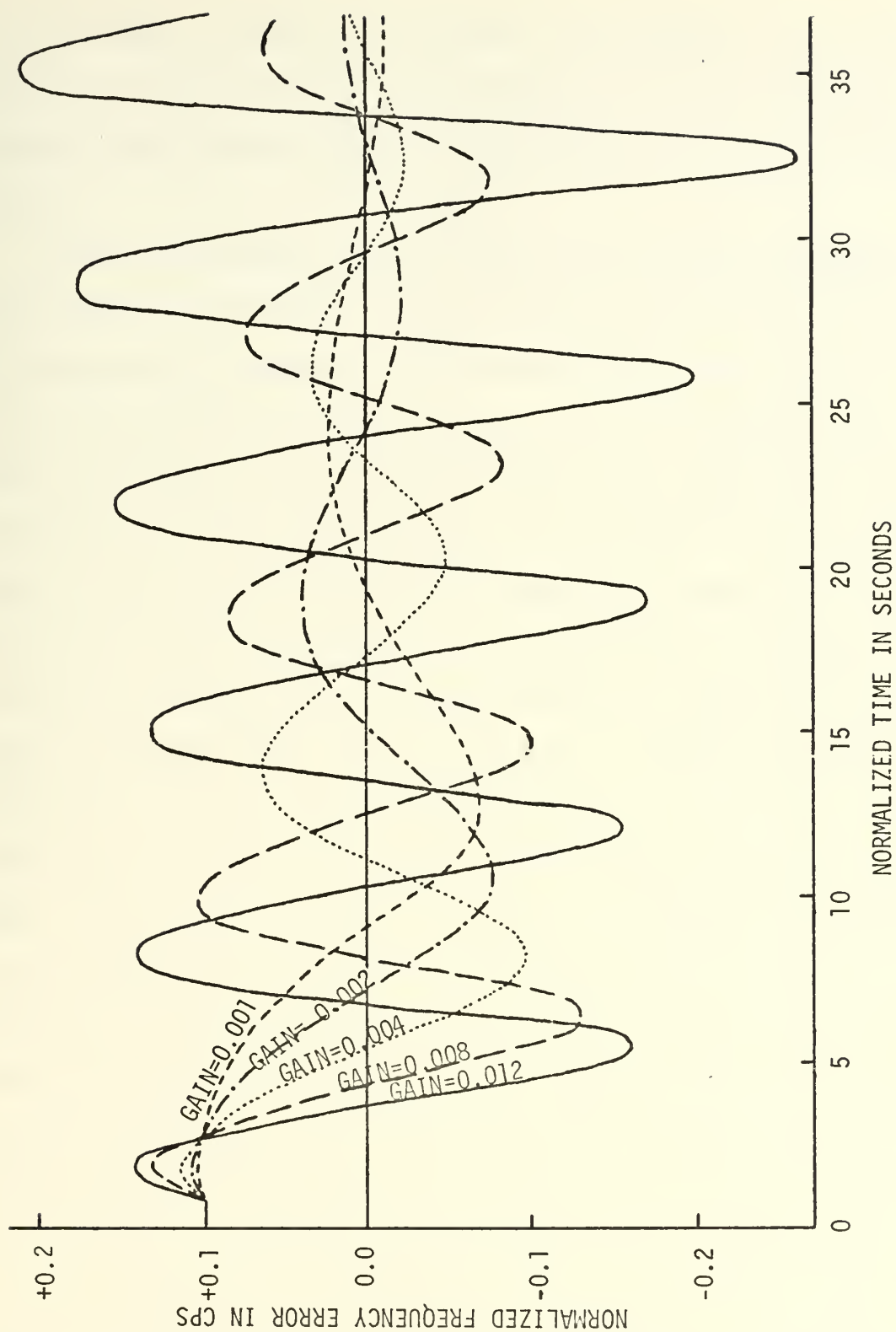


Figure V-D-1. Frequency Error as a Function of Time for the R-S Nonlinear Phase Comparator with Track and Hold for an Input Frequency of 1.1 cps, Initial Phase of 90 Degrees, and TC of 5.0.

various values of loop gain as indicated in the Figure. It is seen in Figure V-D-1 that the system became unstable for values of gain slightly greater than 0.008, due primarily to the action of the track and hold circuit.

For most performance criteria, the R-S nonlinear phase comparator with track and hold did not live up to expectations, and the compounding of nonlinearities resulted in a circuit operation that was quite arbitrary and unpredictable in that slight variations in either the gain or the initial conditions of frequency or phase would often cause erratic variations in system performance which were difficult to explain. One aspect of circuit operation which did agree with expected results was that in the steady state condition the instantaneous VCO frequency variation did approach zero. Another performance objective that not only met with a limited degree of success but also concurred with expected results was that for a fixed frequency and gain the variation of lock performance was relatively constant over the complete range of input phase. This uniform lock time as a function of phase was due primarily to the action of the nonlinear phase comparator and its ability to increase the system gain for increases in phase deviation. One area in which the circuit under study appeared to compromise between the characteristics of its constituent parts was that the combined circuit was able to attain lock even after cycle skipping had occurred. The ability to skip cycles and still lock was not present for the case of the normal R-S phase comparator with track and hold, and therefore this added capability must have been due to the action of the nonlinear phase comparator. However, the time to acquire lock took longer than for the R-S nonlinear circuit alone.

It was discovered that very little advantage has been gained by the combination of the R-S nonlinear phase comparator with the track and hold circuit, and both the family of curves showing lock time as a function of frequency and the curves of seize frequency as a function of phase showed such unmethodical variations as to indicate that it would be impractical to employ this circuit in actual applications.

E. TRIGGER PHASE COMPARATOR

The advantage of having a phase-locked loop system which would operate satisfactorily in the event the input signal were interrupted has been previously alluded to several times in this treatise. When discussing the R-S phase comparator it was mentioned that this capability to operate in the absence of an input signal could be incorporated into the system by connecting the VCO signal to a 'count' terminal on the phase comparator flip-flop. An easier and more effective way of obtaining this zero-input capability will be described in this subsection, and the circuit implementation will be called a trigger phase comparator. The trigger phase comparator is new to the field of phase-locked loops, and no reference to this particular form of phase comparator has been found in previous literature on the subject.

The trigger phase comparator was constructed using a trigger flip-flop with output states of equal amplitude but opposite polarity. The flip-flop was connected so that a pulse from either the input pulse train or the VCO pulse train would trigger or reverse the state of the flip-flop, and the circuit action made no distinction as to the source of the input pulse. This was in contrast to the R-S phase comparator where the flip-flop responded differently to the signals from each pulse train. The actual analog simulation procedure used was to pass the input and VCO

pulses through an OR gate which yielded a single pulse train with all the pulses of both the input and VCO. This composite pulse train was then applied to the input of a conventional trigger flip-flop. The same effect was obtained in the digital simulation using logic statements.

It can now be seen why the trigger flip-flop is able to operate even in the absence of an input signal. If no input signal is present then the pulse train to the flip-flop will contain only pulses from the VCO, and the flip-flop output will alternate between positive and negative values at a frequency of one half the VCO frequency. Nevertheless, the average output of the flip-flop will be zero if the average is taken over any two periods of the VCO waveform, and since the average output of the phase comparator is zero, the average VCO frequency will remain unchanged from the frequency at which the VCO was operating when the input signal was lost. This zero-input capability also allows the circuit to be activated in a standby status with the VCO operating at its center frequency prior to the arrival of the input pulse train. There is one difference in the operating characteristics of the circuit with and without an input signal, and that is that in the absence of the input signal the flip-flop output remains longer in each state prior to changing states than it does when an input signal is present. This means that the control voltage applied from the phase comparator through the filter to the VCO makes greater excursions from its average value, and although the average output of the VCO remains unchanged, the instantaneous frequency variation is approximately double what it would be if the input signal had been present. However, this increased instantaneous frequency variation in the absence of an input signal is identical to that which would be obtained if the normal R-S phase comparator were used with the VCO signal applied to a 'count' input.

Under normal operating conditions with both the input and the VCO signals present, the operation of the trigger phase comparator is identical with that of the R-S phase comparator up to the point where cycle skipping occurs. This is evident since if the initial state of the trigger flip-flop is properly set at the beginning of circuit operation so that with the initiation of the VCO circuit at time zero the output of the flip-flop is negative, then the trigger flip-flop will pass through the identically same series of states of positive and negative voltage as would the R-S phase comparator. However, when cycle skipping occurs the systems react differently as will be demonstrated later in this subsection. Since the trigger and the R-S phase comparator respond alike until cycle skipping, then the seize frequency of the trigger phase comparator should be identical with that of the R-S phase comparator. Experimentation has confirmed this expectation, and the curves of seize frequency versus phase for the trigger circuit corresponded exactly with the curves of seize frequency for the R-S phase comparator shown in Figure IV-E-3.

In order to further investigate the characteristics of the trigger phase comparator, a plot was made using data obtained with the digital simulation to show the variation of normalized frequency-lock time as a function of normalized input frequency for a gain of 0.002 and an input phase of 180 degrees. A second plot was made under identical operating conditions but employing the R-S phase comparator, and these curves for both the trigger and R-S phase comparator are shown in Figure V-E-1. From the curves of Figure V-E-1 it is seen that the frequency-lock times of both phase comparator circuits are identical within certain limits of deviation of the input frequency, after which the trigger phase comparator demonstrates superior performance over the range of input

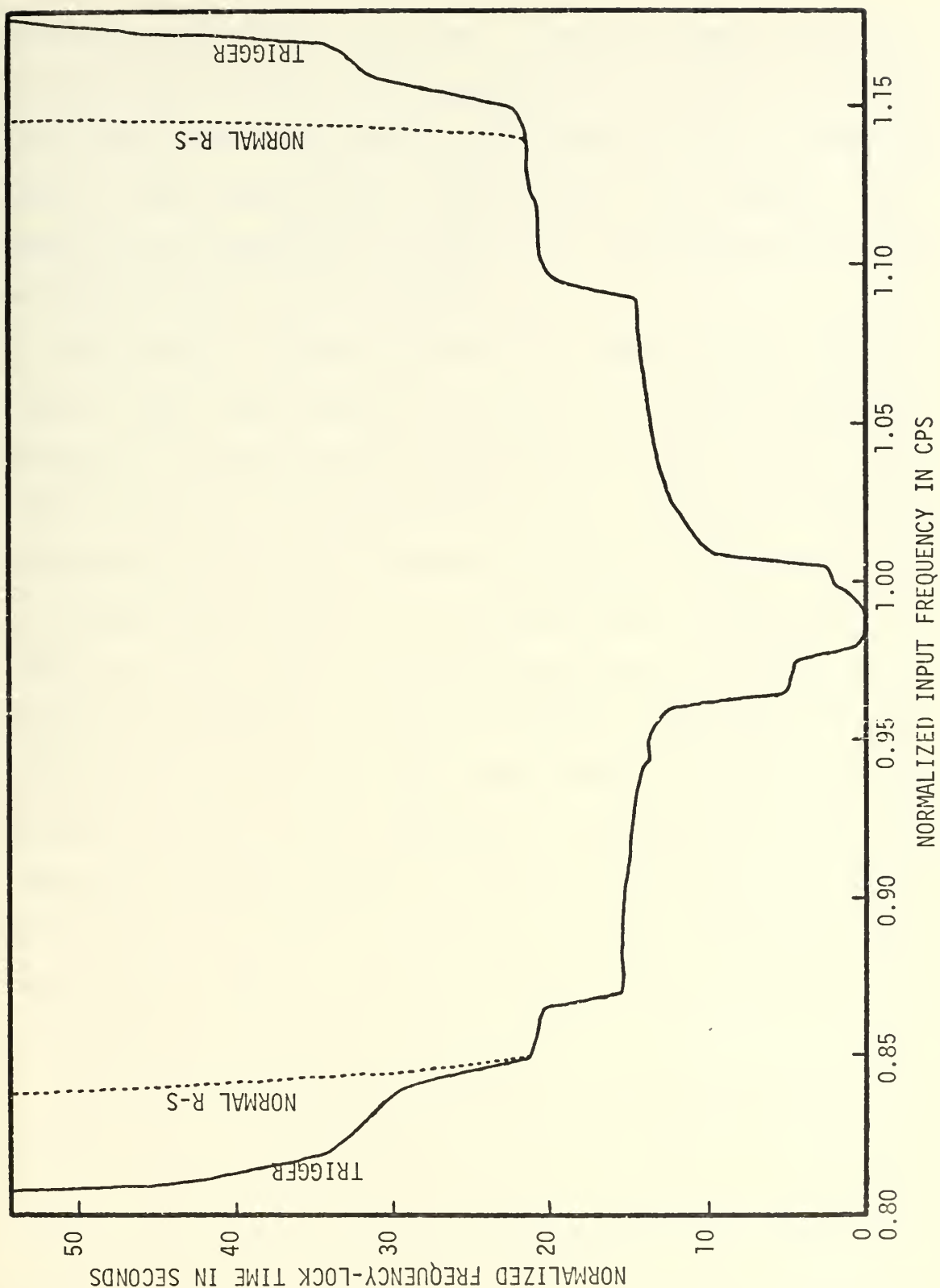


Figure V-E-1. Frequency-Lock Time as a Function of Input Frequency for the Trigger and the Normal R-S Phase Comparators for a Gain of 0.002 and an initial Phase of 180 Degrees.

frequencies exhibited in this figure. A detailed examination of the printed digital output revealed that the frequency offset at which the lock times of the trigger and R-S phase comparators begin to differ was also the same frequency at which cycle skipping first occurred. This confirmed the statement made previously that the system operation would be identical prior to cycle skipping.

An explanation will now be given with the help of Figure V-E-2 as to why the trigger phase comparator outperforms the normal R-S phase comparator for frequencies where cycle skipping has begun to occur. The curves of Figure V-E-2 show simultaneously as a function of time some of the waveforms which exist in the phase-locked loop simulation when using the trigger phase comparator. The waveforms shown include those of the input pulse train in part (a), the VCO pulse train in part (b), the average and instantaneous normalized frequency error using the trigger flip-flop in part (c), the trigger phase comparator output in part (d), followed in part (e) by the waveform which would appear at the output of the normal R-S phase comparator if the signals of parts (a) and (b) had been applied. The particular operating conditions portrayed in Figure V-E-2 are for a normalized input frequency of 1.17 cps, an initial phase of 90 degrees, and a gain of 0.002.

An examination of parts (a) and (b) of Figure V-E-2 shows that cycle skipping occurs at the sixth and the twentieth pulse of the input pulse train. This cycle skipping is reflected in the phase comparator outputs shown in parts (d) and (e) for the trigger and R-S phase comparators respectively, but the effects of the cycle skipping are quite different between the outputs of these two phase comparators. The average value of the normal R-S phase comparator output voltage taken over one period of the input signal makes an abrupt transition when a cycle is skipped;

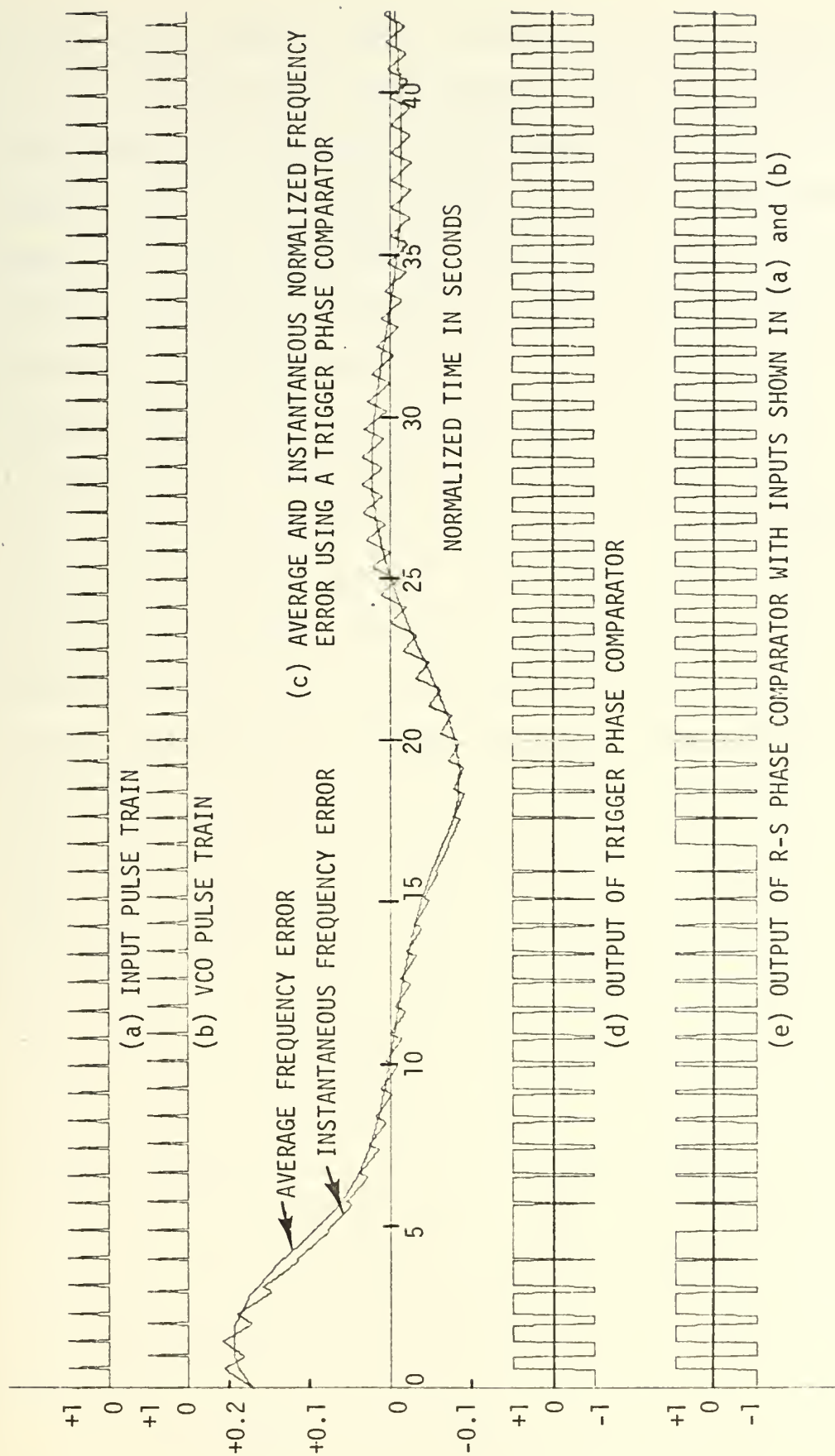


Figure V-E-2. Operating Characteristics of a Phase-Locked Loop with a Normalized Input Frequency of 1.17 cps, Initial Phase of 90 Degrees, and a Gain of 0.002.

and, since this control voltage is applied to the VCO through the filter, it can be seen that the voltage which was driving the system toward lock would suddenly be reversed and now drive the system away from lock. This sudden reversal of the control voltage to the VCO is what caused the sharp cusp at each skipped cycle as seen in the curves of VCO control voltage as a function of time shown in Figure IV-A-5, and the change in VCO control voltage in turn caused the corresponding rapid increase in frequency error which occurred at the time of a skipped cycle as shown in Figure IV-B-4. From Figure IV-B-4 it is seen that after each skipped cycle the R-S phase comparator actually drives the system away from lock for a period of time, and thus the overall lock time of the system is significantly increased. The average output voltage of the trigger phase comparator shown in part (d) of Figure V-E-2 does not exhibit the reverse in polarity which was seen to exist for the R-S phase comparator, since now each individual pulse reverses the output of the phase comparator while with the R-S phase comparator whenever a cycle was skipped one pulse passed through without affecting the state of the flip-flop. Since no abrupt change in polarity occurs at a skipped cycle for the trigger phase comparator, the VCO is not suddenly driven away from lock, and instead, the system proceeds on smoothly to attain lock as shown in part (c) of Figure V-E-2 without sudden reversals or cusps in the curve of average frequency error. Thus, once cycle skipping takes place the trigger phase comparator attains lock faster than the normal R-S phase comparator due to its ability to operate without some of the transients which would be introduced into the system if the R-S phase comparator had been used.

It has been shown in Figure V-E-1 that the trigger phase comparator exhibits reduced lock times for a fixed value of phase and for frequencies

just beyond the seize frequency. It was then necessary to determine if this phenomenon existed for all values of phase. The frequency-lock time of both the trigger and R-S phase comparator was computed for each five degrees of phase for an input frequency of 1.15 cps, which is just beyond the seize frequency, and the results are shown in Figure V-E-3. For all values of phase the trigger phase comparator exhibited significantly reduced lock times which were on the order of about 60 percent of the lock times of the R-S phase comparator. In addition, lock times of the trigger phase comparator showed much less variation with phase than the lock times of the R-S phase comparator, which varied widely for minor changes in phase as a result of changes in the number of skipped cycles.

Experimental investigation of the trigger phase comparator operation for wide variations of the input frequency indicated that its performance was similar to the R-S phase comparator in that no limiting lock range could be found within the capabilities of either the analog or digital simulations, and although the lock times became excessively long as the frequency deviations increased, the system would always attain lock. From Figure V-E-1 it was observed that for frequency deviations less than the seize frequency the R-S and trigger phase comparator's frequency-lock times were identical, and for frequency deviations greater than the seize frequency the trigger phase comparator's lock times were less than those of the R-S phase comparator. However, for very large frequency deviations the relationships changed again, and then the lock time of the R-S phase comparator became less than that of the trigger phase comparator.

The trigger phase comparator was also substituted into the R-S nonlinear circuit described in Subsection V, B to make a nonlinear trigger circuit. The results of this circuit combination will not be discussed in detail in this report, since the relationships between the trigger

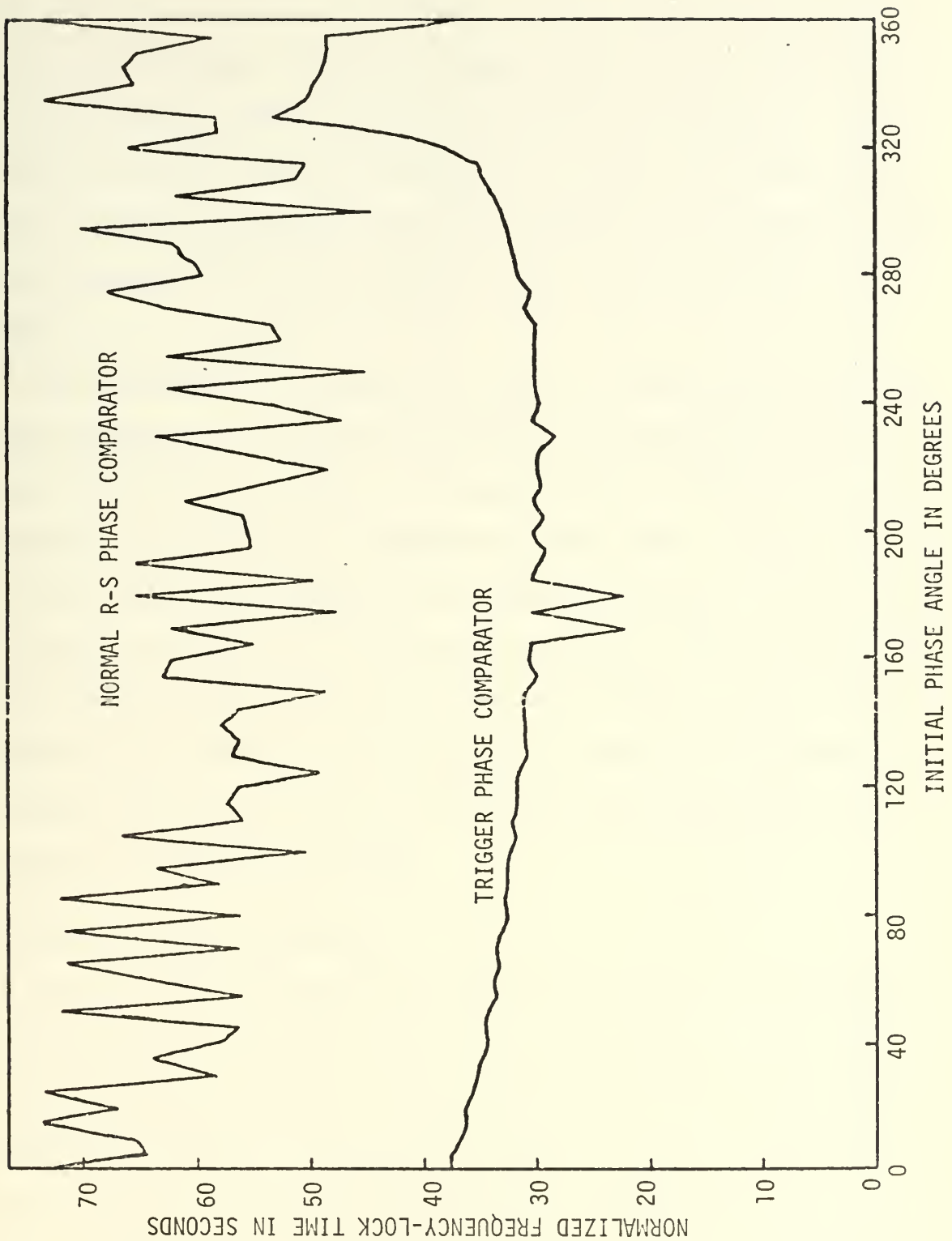


Figure V-E-3. Frequency-Lock Time as a Function of Phase for Both the Trigger and Normal R-S Phase Comparators for a Gain of 0.002 and an Input Frequency of 1.15 cps.

nonlinear circuit and the R-S nonlinear circuit were analogous to the relationships between the linear trigger circuit and the linear R-S circuit which have been discussed in detail in this subsection. The trigger nonlinear circuit was identical with the R-S nonlinear circuit until cycle skipping occurred, and for frequencies just greater than the seize frequency the trigger nonlinear circuit exhibited shorter lock times.

The substitution of a trigger flip-flop for the R-S flip-flop in the phase comparator has added to the versatility of the phase-locked loop in that now the circuit is able to continue operating satisfactorily even in the event the input signal is temporarily interrupted. Circuit operation with the trigger phase comparator has remained identical to that of the R-S phase comparator for all frequencies below the seize frequency, but for frequencies just greater than the seize frequency the system performance has been improved. In addition, the trigger phase comparator has retained the important capability of the R-S phase comparator in that it also has an unlimited lock range.

F. ADDITIVE PHASE COMPARATOR

Another circuit configuration which will be referred to by the descriptive name of additive phase comparator will be studied in this section. The additive phase comparator also belongs to the family of sawtooth phase comparators because of the linear relationship between its average output over one cycle and the phase relationship of the signals during that cycle. The operation of the additive phase comparator can best be described with the help of Figure V-F-1 which demonstrates how the system components function. A pulse from the input signal turns on two different independent flip-flops, one of which has an amplitude of + 1.0 volts and is designed

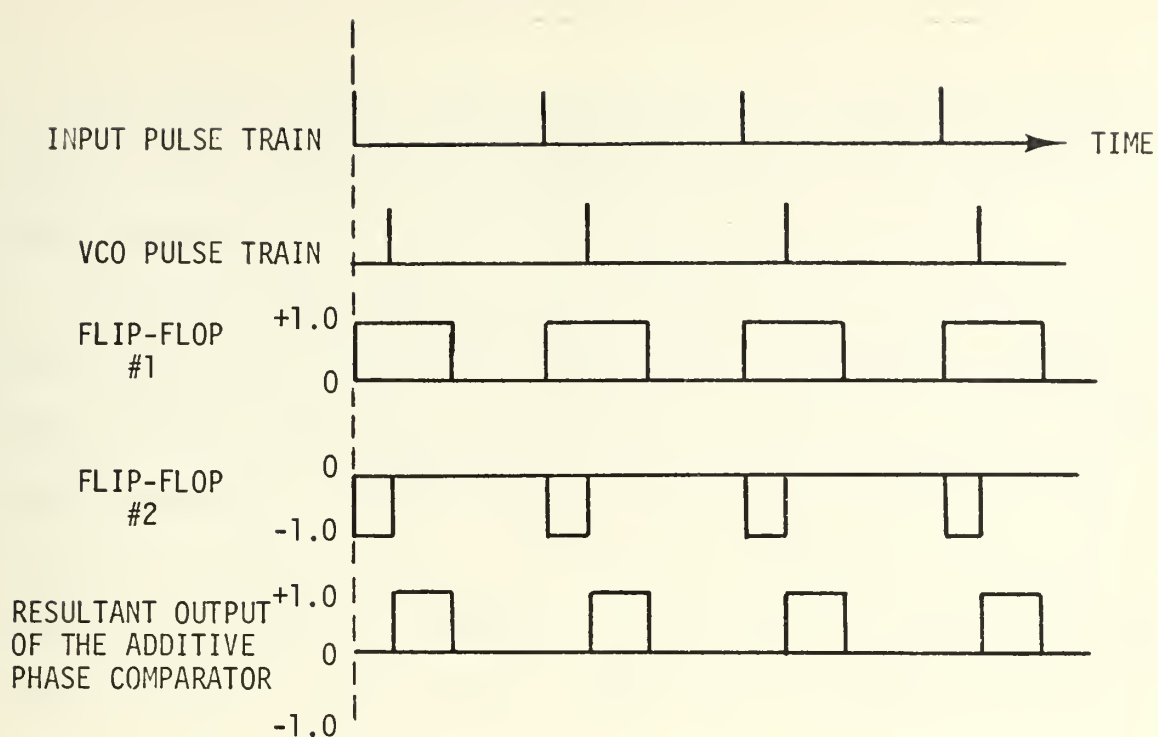


Figure V-F-1. Operation of the Additive Phase Comparator.

to remain in an on condition for a period of time corresponding to exactly one half the period of the VCO free-running frequency. The other flip-flop has an amplitude of -1.0 volts, and is also turned on by the input signal and remains on until the arrival of a pulse from the VCO. The overall phase comparator output is obtained by adding the output of the two separate flip-flops. The output of the phase comparator averaged over one period of the input signal can then be expressed as a function of the normalized phase angle ϕ_{on} by which the VCO lags the input signal as

$$f(\phi_{on}) = 0.5 - \phi_{on}. \quad (V-f-1)$$

Equation V-f-1 is only valid for the condition where the input frequency equals the VCO free-running frequency. The normalized phase comparator gain $\frac{df(\phi_{on})}{d\phi_{on}}$ can be obtained from Equation V-f-1 and is -1.0. It should

be noted that the additive phase comparator gain is only one half the magnitude and is also of opposite polarity to that of the normal R-S phase comparator.

The additive phase comparator was inserted into the analog program by the use of both a delay flip-flop and an R-S flip-flop, and simple logic statements were used to incorporate the additive circuit into the digital simulation. In both the analog and digital simulation it was necessary to invert the polarity of the filter output due to the sign inversion of the phase comparator, and it was also necessary to increase the gain of the loop amplifier by a factor of 2.0 to make the overall loop gain conform to that of Equation III-a-13.

The normalized frequency error of the additive phase comparator as a function of time for a normalized input frequency of 1.1 cps, phase angle of 90 degrees, and for various values of loop gain is plotted in Figure V-F-2. From this figure it can be seen that the additive phase comparator is not plagued with serious problems of instability, and its high gain performance appears quite similar to that of the normal R-S phase comparator. When the average and instantaneous phase error of the additive phase comparator is plotted as a function of time for an input frequency of 1.0 cps and an input phase of 90 degrees, the curves are as shown in Figure V-F-3. These curves show that for the additive phase comparator the instantaneous frequency variation in steady state has been reduced to zero due to the phase comparator action described in Figure V-F-1, where it can be observed that the steady state condition will exist only when the input and VCO signals differ by 180 degrees, thereby resulting in complete cancellation of the two flip-flop voltages and yielding a constant zero output from the phase comparator. A zero

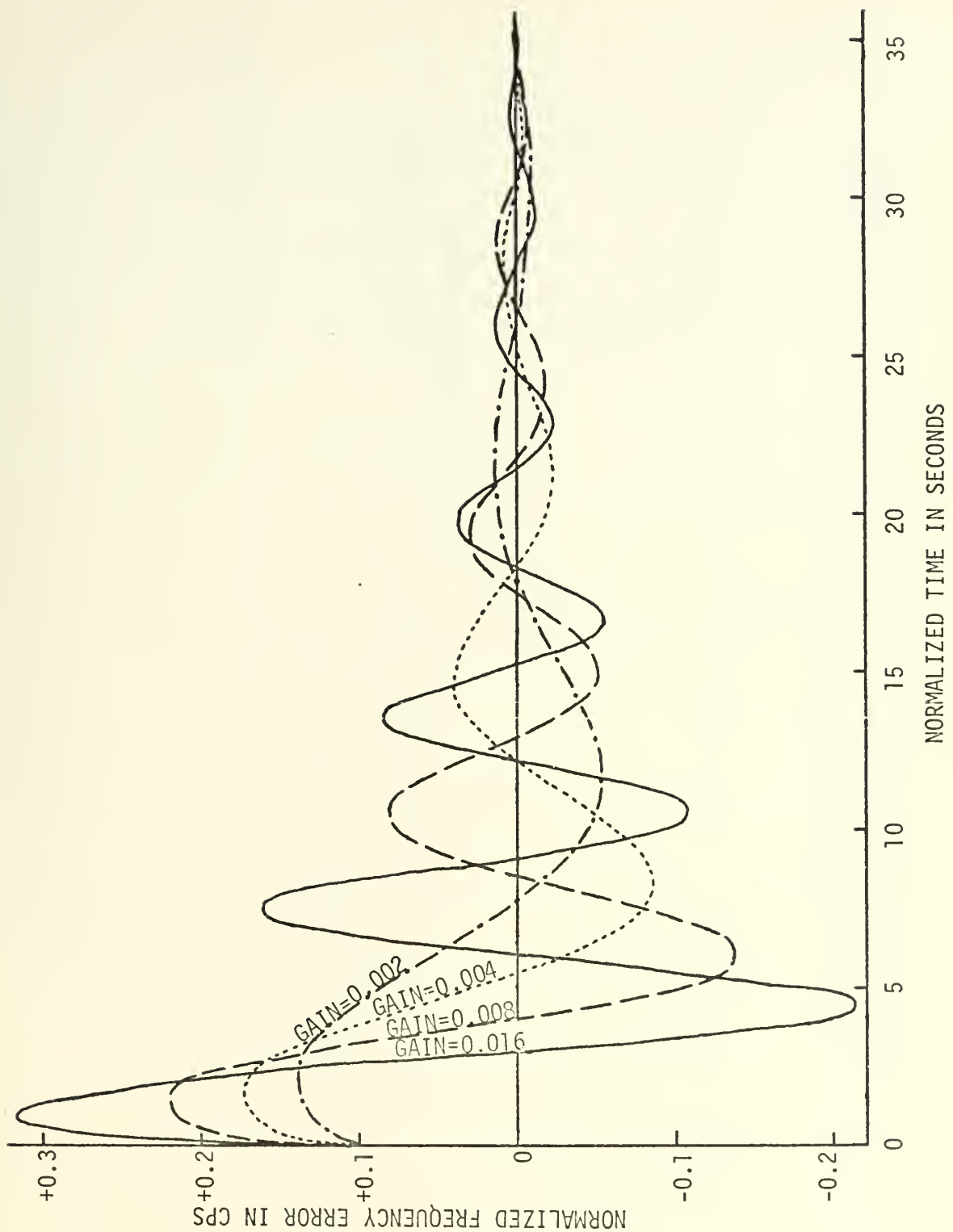


Figure V-F-2. Frequency Error as a Function of Time for the Additive Phase Comparator with an Input Frequency of 1.1 cps and an Initial Phase of 90 Degrees.

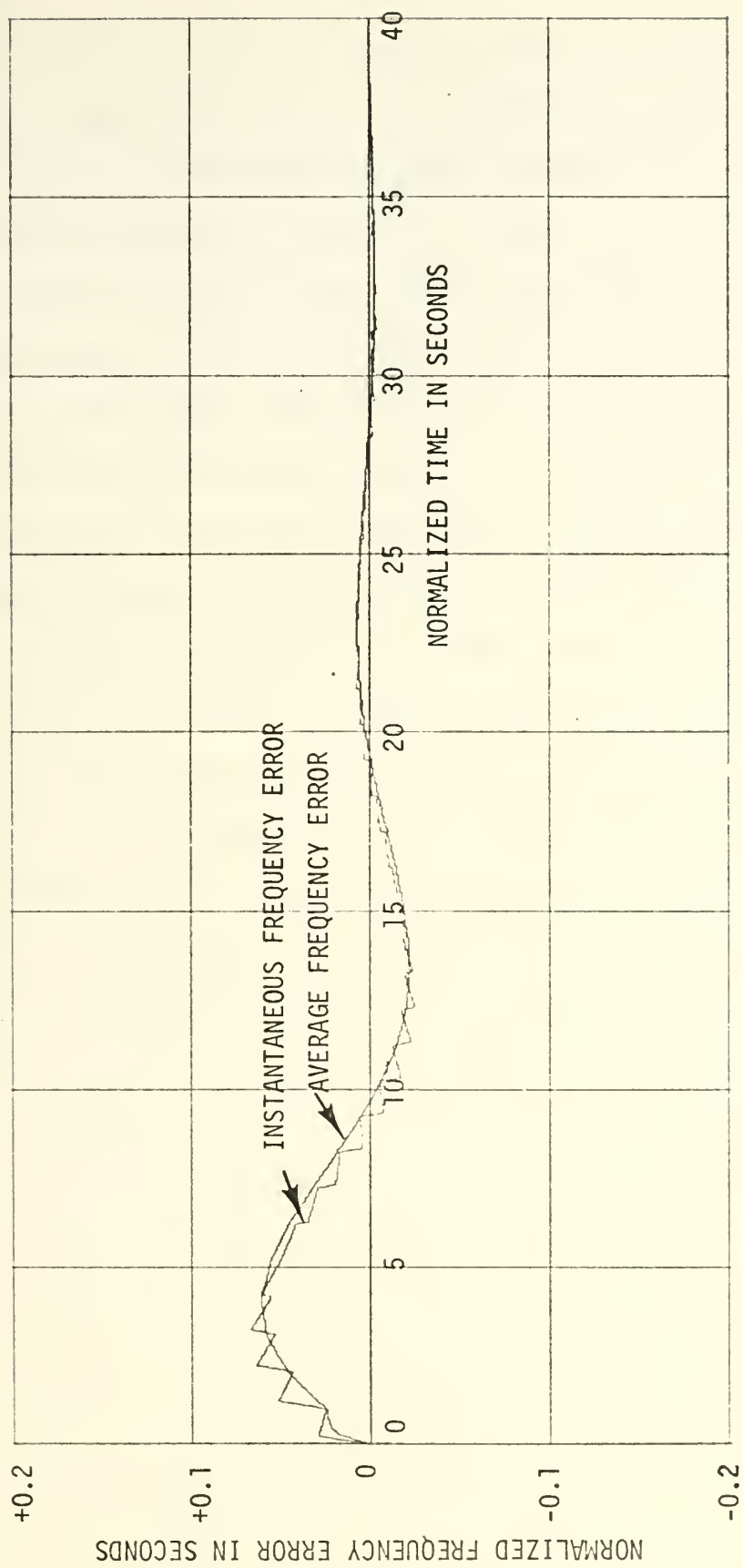


Figure V-F-3. Average and Instantaneous Frequency Error as a Function of Time for the Additive Phase Comparator with an Input Frequency of 1.0 cps, Initial Phase of 90 Degrees, and a Gain of 0.002.

instantaneous steady state frequency output had been obtained previously in the R-S phase comparator by the addition of a track and hold circuit, but in the case of the additive phase comparator the same results were accomplished through the action of the phase comparator circuit alone, and no additional modifications were required outside of the phase comparator unit. Even while the system is proceeding to lock, the output of the additive phase comparator is such that during any given cycle of the input signal the output voltage is either zero or of a fixed polarity as determined by the phase relationship, and the output does not alternate between positive and negative values during any cycle of the input pulse period as does the R-S phase comparator.

In order to further investigate the operating characteristics of the additive phase comparator, the family of curves given in Figure V-F-4 was made to show the normalized frequency-lock time as a function of the normalized input frequency for a gain of 0.002 and for three different values of input phase. The circled points at the end of the curves in this figure represent the limiting frequencies for which the system would attain lock, and for frequencies beyond these limiting values the system would not attain lock even for extended periods of operation. From Figure V-F-4 it is seen that the lock range is greater for frequencies lower than the normal VCO frequency. The frequency-lock times for the system when operating with an input frequency a fixed amount below the VCO frequency are also less than those for the system when operating with an input frequency the same amount above the VCO frequency. These observations suggest that there exists a variation of system gain as a function of frequency.

In order to investigate the system gain characteristics as a function of input frequency it is helpful to return to Figure V-F-1 and note that

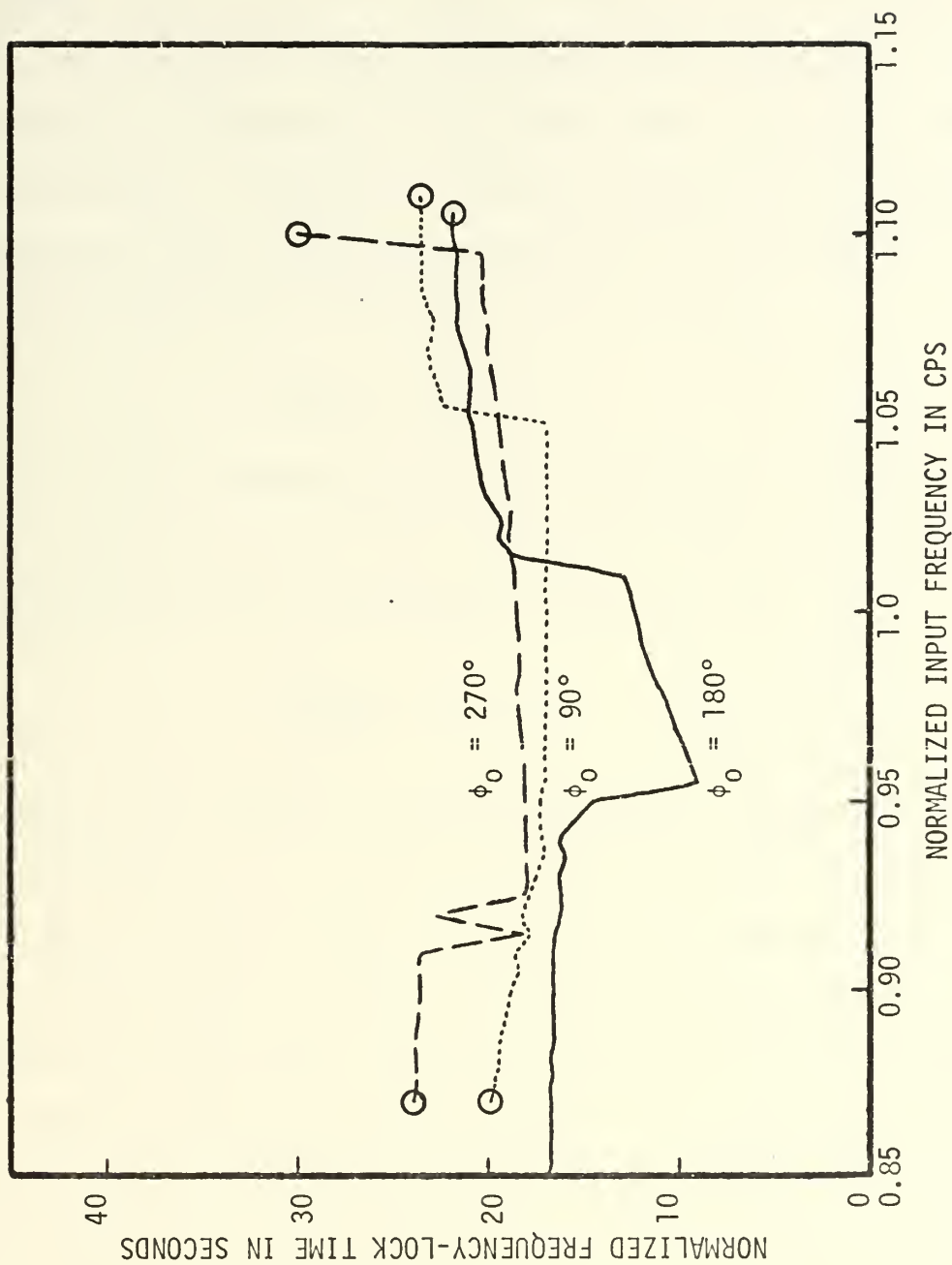


Figure V-F-4. Frequency-Lock Time as a Function of Input Frequency for the Additive Phase Comparator with a Gain of 0.002.

the output of the first flip-flop has a fixed pulse duration which is designed to be one half the period of the VCO center frequency. As the input pulse changes frequency the length of the fixed pulse is not altered, but the operation of the overall phase comparator is affected. If the effects of variations in the input frequency are considered, then the average output of the phase comparator can be expressed as a function of the normalized input phase and normalized time as

$$f(\phi_{on}) = 0.5 - t_1 \quad , \quad (V-f-2)$$

where the time t_1 equals ϕ_{on} PD and is the time of arrival of the VCO pulse using the arrival of the input pulse as time zero. Equation V-f-2 can be solved for the system gain which is given as

$$\frac{df(\phi_{on})}{d\phi_{on}} = - PD \quad . \quad (V-f-3)$$

Equation V-f-3 indicates that the system gain is independent of the phase relationships, but is an inverse function of the input frequency. A plot of $f(\phi_{on})$ is shown in Figure V-F-5 for various values of input frequency, and in this figure the slope of the curves, which corresponds to the system gain, can be seen to vary as a function of input frequency.

Another characteristic of the additive phase comparator which has not been experienced with any of the other phase comparators is the existence of a steady state phase error. In steady state operation the output of the phase comparator over any given period of the input signal must be zero, or else the VCO would be driven off its steady state value. If the phase comparator output is to be zero then the operating condition must be at that point where the curve of $f(\phi_{on})$ intersects the ϕ_{on} axis at zero magnitude. For an input frequency of 1.0 cps this intersection occurs at a ϕ_{on} of 0.5 which corresponds to a phase of 180. However, as the

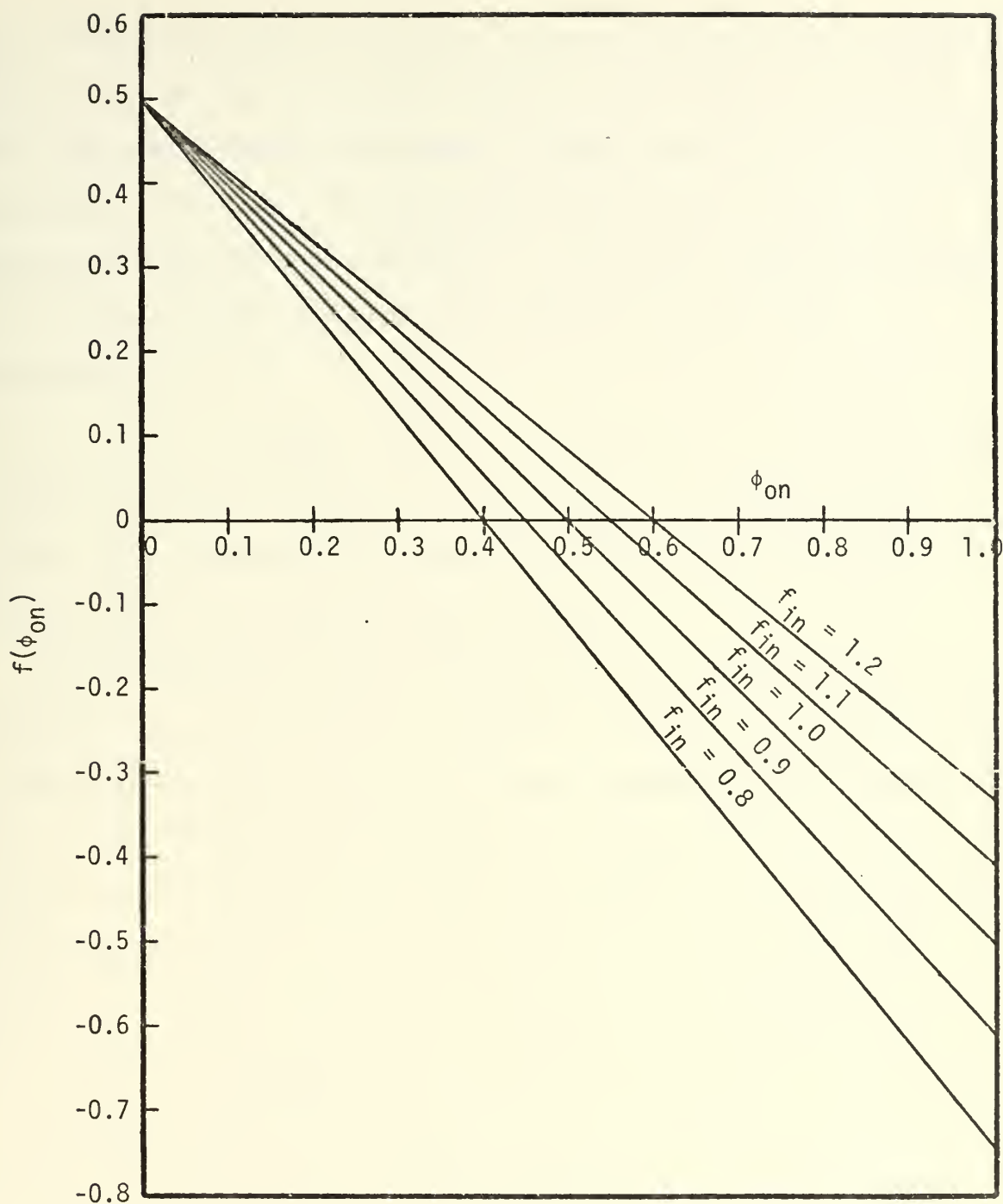


Figure V-F-5. Average Phase Comparator Output as a Function of the Normalized Phase ϕ_{on} for the Additive Phase Comparator for Various Values of the Input Frequency.

input frequency varies, this point of intersection shifts from the 180 degree position, and for any input frequency other than 1.0 cps there will always be a steady state phase error when using the additive phase comparator. The amount of this steady state phase error ϕ_{ess} can be determined graphically from Figure V-F-5, and can be expressed in degrees as a function of the normalized input frequency by the linear relationship.

$$\phi_{ess} = - 180.0 + 180.0(f_{in}) . \quad (V-f-4)$$

A normalized input frequency of 1.1 cps yields a phase error of 18.0 degrees. The presence of this steady state phase error is one of the disadvantages of the additive phase comparator.

Having determined the gain characteristics as a function of input frequency it is now possible to return for a closer look at the curves of frequency-lock time as a function of input frequency shown in Figure V-F-4. The increased gain with decreased frequency explains the occurrence of lower lock times and longer lock ranges at low input frequencies. An additional observation can also be made in that the curves show a shorter lock time at the low frequencies for a phase of 90 degrees than for a phase of 270 degrees, and an approximate reversal of this phenomenon is observed at the higher frequencies. This difference in lock times is probably due to the shift in steady state phase to a lower phase angle for the lower input frequencies, and to a higher phase angle for the higher input frequencies. Therefore, for a lower input frequency a signal with an initial phase angle of 270 degrees and one with an initial phase angle of 90 degrees are not equidistant from their steady state value, and since the signal with the 90 degree phase angle is closer to its final value it should be expected to lock first, which is exactly the phenomenon observed in Figure V-F-4.

It has also been determined for the additive phase comparator that, with few exceptions, if the system skips one cycle it will never lock. In fact, for the data shown in Figure V-F-4 there was only one frequency which locked after skipping a single cycle, and that was for a normalized input frequency of 1.10 cps and an initial phase of 270 degrees. In this respect the additive phase comparator was much like the R-S phase comparator with track and hold. A resemblance between the sampling characteristics of the track and hold circuit and the additive phase comparator can also be seen from the circuit operation portrayed earlier in Figure V-F-1. The output pulses from the phase comparator are fed to an integrator in the filter circuit, and the output of the integrator will vary or track the phase comparator output only during those times when there is a pulse present at the phase comparator output. For the remaining portion of the period of the input signal the integrator output will simply hold the last value received from the phase comparator output, since it is receiving no further signal to integrate. Thus the lead-lag filter experiences an input voltage which is very much like the output of a track and hold circuit; and, depending upon the phase relationship, the operation can vary from only a very short tracking interval with a long holding interval to a tracking interval which approaches one half of the period of the input signal with a corresponding holding time equal to the remaining one half of the input period. Therefore, since the additive phase comparator possesses some of the characteristics of a track and hold circuit it is not unexpected that its response also contains some similarity to the R-S phase comparator with a track and hold circuit added, even though these attributes may be present to a much lesser degree.

The variation of the normalized frequency-lock time as a function of phase is shown in Figure V-F-6 for a gain of 0.002 and for three values of normalized input frequency. These curves also conform to the data shown in Figure V-F-5 concerning the variation of gain with frequency, since the curve for f_{in} of 0.9 cps almost always exhibits a shorter time to lock than the curve for f_{in} of 1.1 cps, even though the frequency in both cases differs from the normal VCO frequency by the same amount. This difference in lock time occurs because of the increase in gain for a decrease in input frequency. In fact, there is not even a significant difference in lock times between the curve for an input frequency of 0.9 cps and the curve for an input frequency of 1.0 cps, since the increase in gain at the lower frequency tends to offset the effect of the deviation in frequency. Another item to be noted in Figure V-F-6 is that although there is a tendency for the system to exhibit a longer lock time when the phase varies greatly from its steady state value, there is not as great a variation of lock time with phase as for the R-S phase comparator with track and hold. A comparison of the curves of frequency-lock time versus phase for the additive phase comparator and the curves of the R-S phase comparator shown in Figure IV-A-4 reveals that the two have almost identical performance characteristics, except that the additive phase comparator has longer lock times for a region where the phase is very near its steady state value and the input frequency is near 1.0. The additive phase comparator response is still inferior to that of the R-S nonlinear phase comparator for which the lock times are not only significantly less, but the time to lock is almost flat as a function of phase since for the nonlinear case the gain increases for increased phase deviation while for the additive phase comparator the gain remains constant with phase.

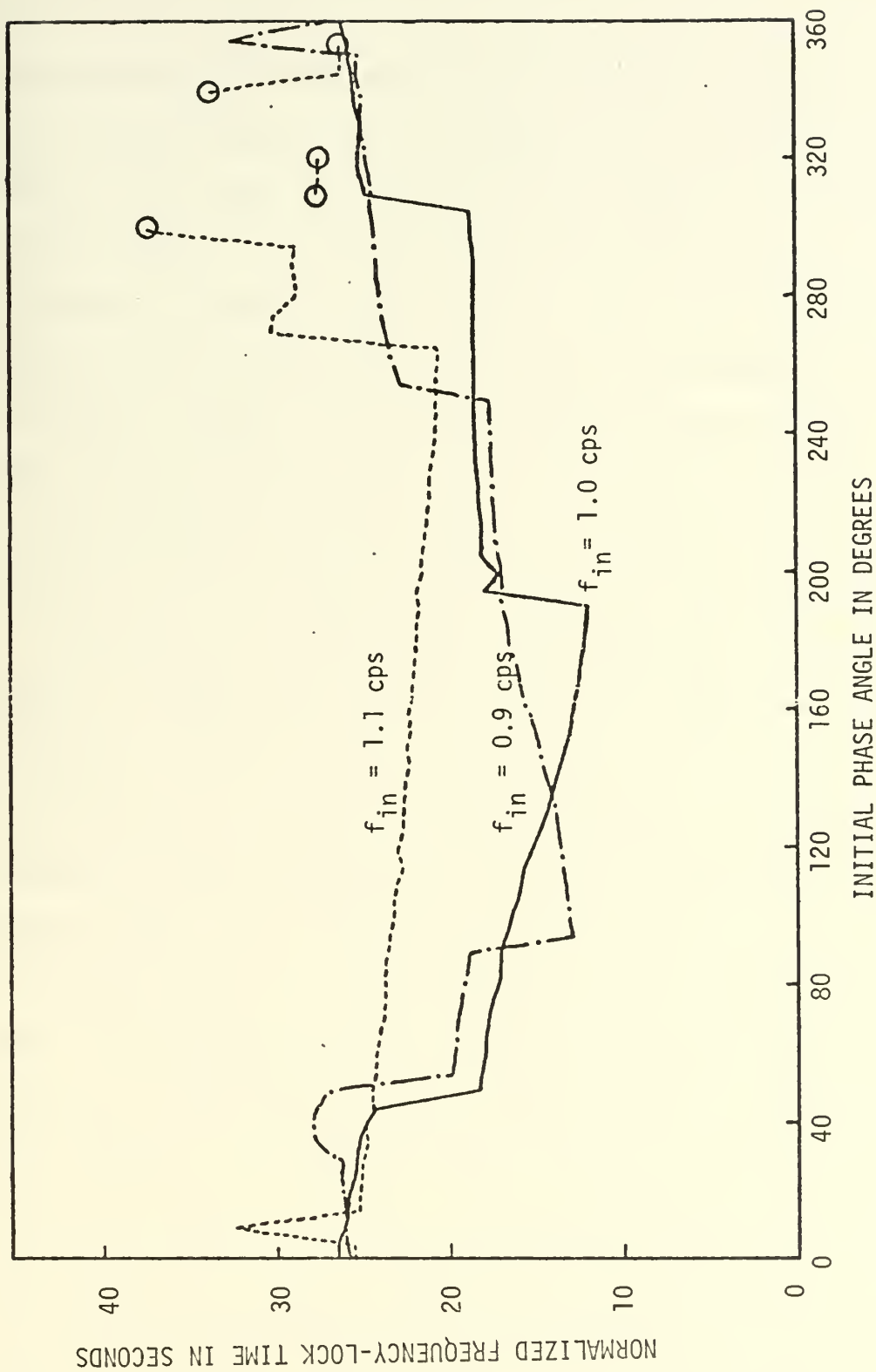


Figure V-F-6. Frequency-Lock Time as a Function of Input Phase Angle for the Additive Phase Comparator with a Gain of 0.002 and for Various Values of the Input Frequency.

For the case of a normalized input frequency of 1.1 cps and for phases of 300 degrees and greater it is seen from Figure V-F-6 that the system sometimes fails to attain lock. It must be remembered that at this frequency the gain has been reduced, and as the phase increases there is little time left for the circuit to adjust itself before cycle skipping occurs. The system first begins to skip cycles at a phase of 270 degrees and skips one cycle before locking, until a phase of 300 degrees where the system skips two cycles in the process of locking. For further increases in phase the system either does not lock at all or skips one cycle and then locks. In no case has the system been observed to lock after skipping more than two cycles, and the probability of ever attaining lock after skipping even one cycle is relatively small.

A good overview of the additive phase comparator's operation is provided in Figure V-F-7 which shows the seize frequency as a function of the input phase for various values of gain. It is seen that for high frequencies the curves tend to indicate a slightly lower range of seize frequency as the phase increases, while for low frequencies the opposite effect is true. This variation in seize frequency is slight and is due to the fact that for some input frequency and phase conditions the initial output of the phase comparator is such as to force the VCO to change frequencies in the wrong direction and thus causes a reduction in the seize frequency. The decrease in gain with increased frequency is also evident from Figure V-F-7 since the range of the seize frequency for high frequencies is much less than that for lower frequencies. With only a few exceptions the curves of seize frequency are also the curves of lock range, but there were a few instances where the system would lock after skipping one or two cycles. The sampling effects of the phase comparator have been shown to be somewhat analogous to that of a track and hold

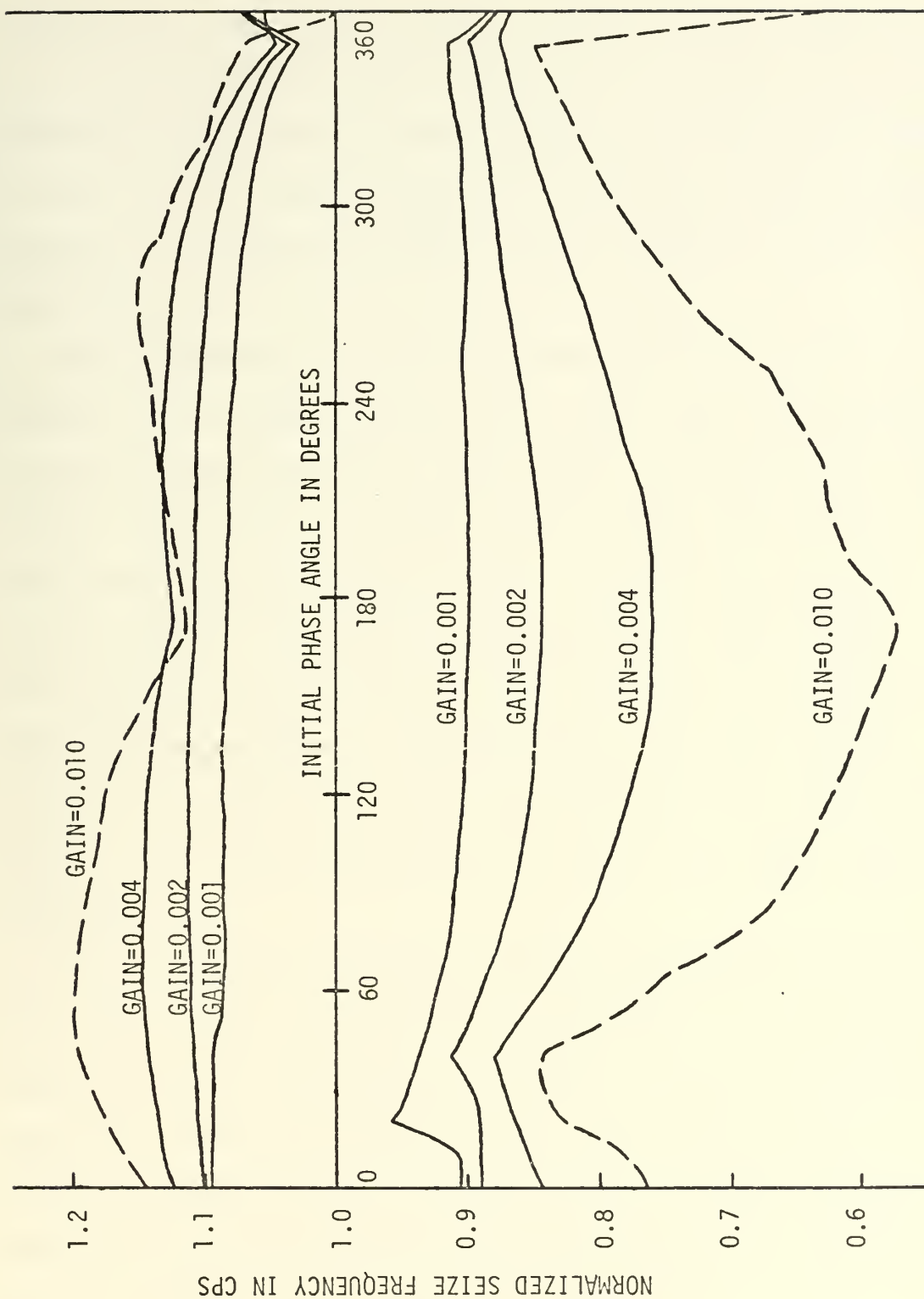


Figure V-F-7. Normalized Seize Frequency as a Function of Initial Phase Angle for the Additive Phase Comparator.

circuit but to a much lesser degree, and there is also a slight similarity between the curves of seize frequency for the additive phase comparator and that of the R-S phase comparator with track and hold shown in Figure V-C-7, in that for both circuits the system tends to become unstable for a lower value of gain than for the normal R-S phase comparator.

One characteristic of the additive phase comparator is its relative insensitivity to temporary losses of the input signal. In the absence of the input signal neither the fixed length flip-flop nor the variable length flip-flop will be activated, and since there will then be no output of the phase comparator the VCO will continue to operate at its current value until the arrival of a pulse from the input waveform. This independent operating ability also allows the circuit to be activated, with the VCO operating in a standby status at its center frequency, prior to the arrival of the input signal, and this mode of operation could be very beneficial when the exact time of arrival of the input signal is not known.

The advantages of the additive phase comparator can be summarized as its ability to operate under steady state conditions without any instantaneous VCO frequency variations, and its capability to operate successfully under zero input conditions. The disadvantages of the system are its limited lock range caused by its relative inability to lock after having skipped a cycle, and its steady state phase error which is dependent upon the frequency deviation.

G. ADDITIVE PHASE COMPARATOR WITH TRACK AND HOLD

Since the effects of adding a track and hold circuit to the R-S phase comparator have been investigated previously, it appeared to be beneficial

to also determine what effects a track and hold circuit would have on the phase-locked loop operation when combined with an additive phase comparator. It was found that the track and hold circuit resulted in similar modifications to circuit performance for the additive phase comparator system as for the R-S phase comparator.

A family of curves showing the average normalized frequency error as a function of normalized time for the additive phase comparator with a track and hold circuit is shown in Figure V-G-1, where it is seen that the limit of stable operation occurs for a gain of about 0.009. The presence of a stability limit at such a low value of gain is in contrast to the normal additive phase comparator which did not experience problems with instability. The reasons for this instability with the track and hold circuit have been explained previously in Subsection V, C. Additional aspects of system response can be observed from the curves of frequency-lock time as a function of initial phase given in Figure V-G-2 and the curves of frequency-lock times as a function of input frequency given in Figure V-G-3. From Figure V-G-2 it is seen that the frequency-lock time increases with increased gain. This increase in lock time with gain is opposite to the effect observed for the normal additive phase comparator, but is similar to what happened when the track and hold circuit was added to the R-S phase comparator. It is also seen from Figure V-G-2 that even for input frequencies which differ from the VCO center frequency by only ten percent the system will fail to lock if the initial phase varies in extent from the steady state phase. The system using the additive phase comparator with track and hold was never observed to lock once cycle skipping had occurred, and the limited lock range observed in Figure V-G-2 was in effect a manifestation of the

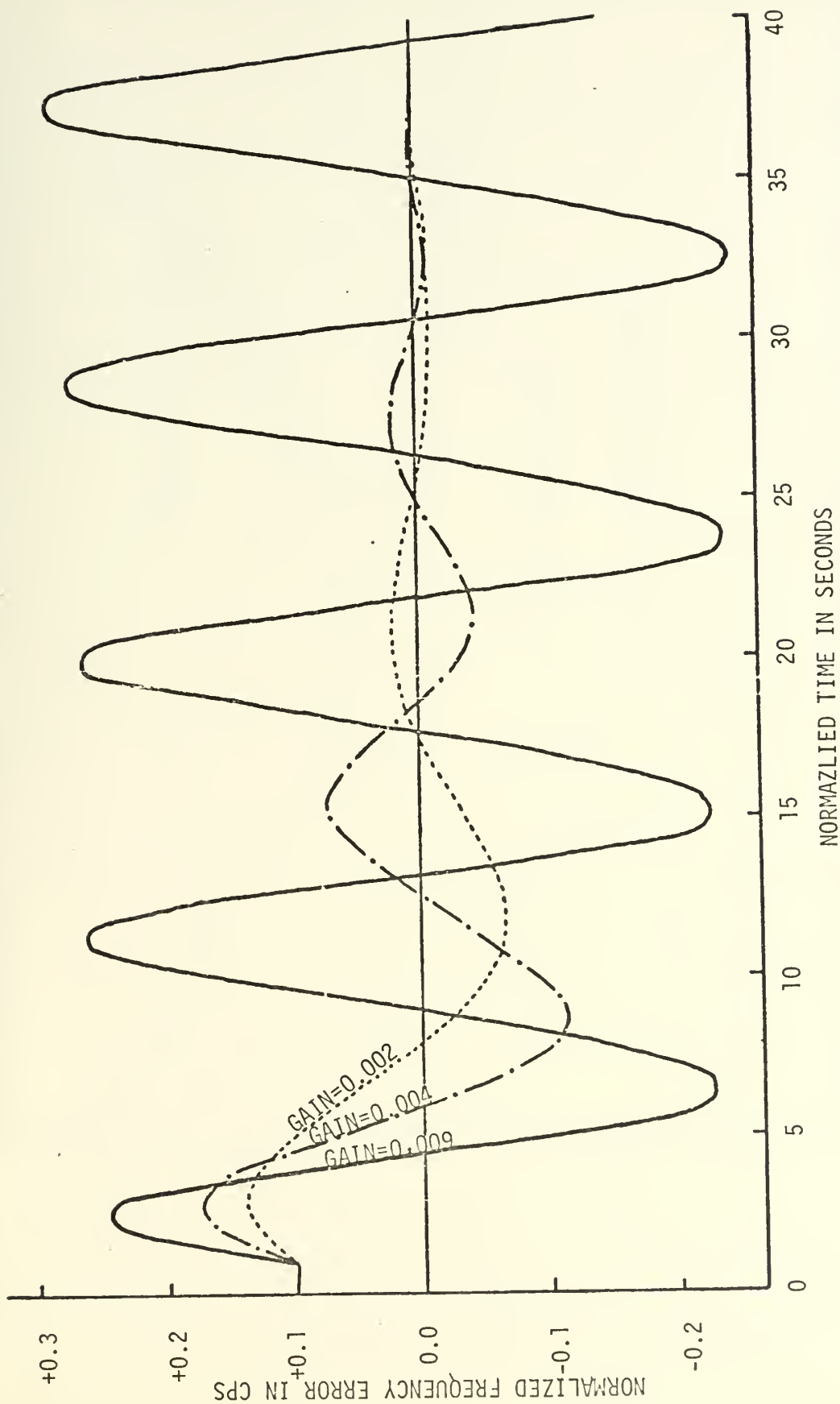


Figure V-G-1. Average Frequency Error as a Function of Time for the Additive Phase Comparator with Track and Hold for an Input Frequency of 1.1 cps, Initial Phase of 90 Degrees, and Gain as Specified on Each Curve.

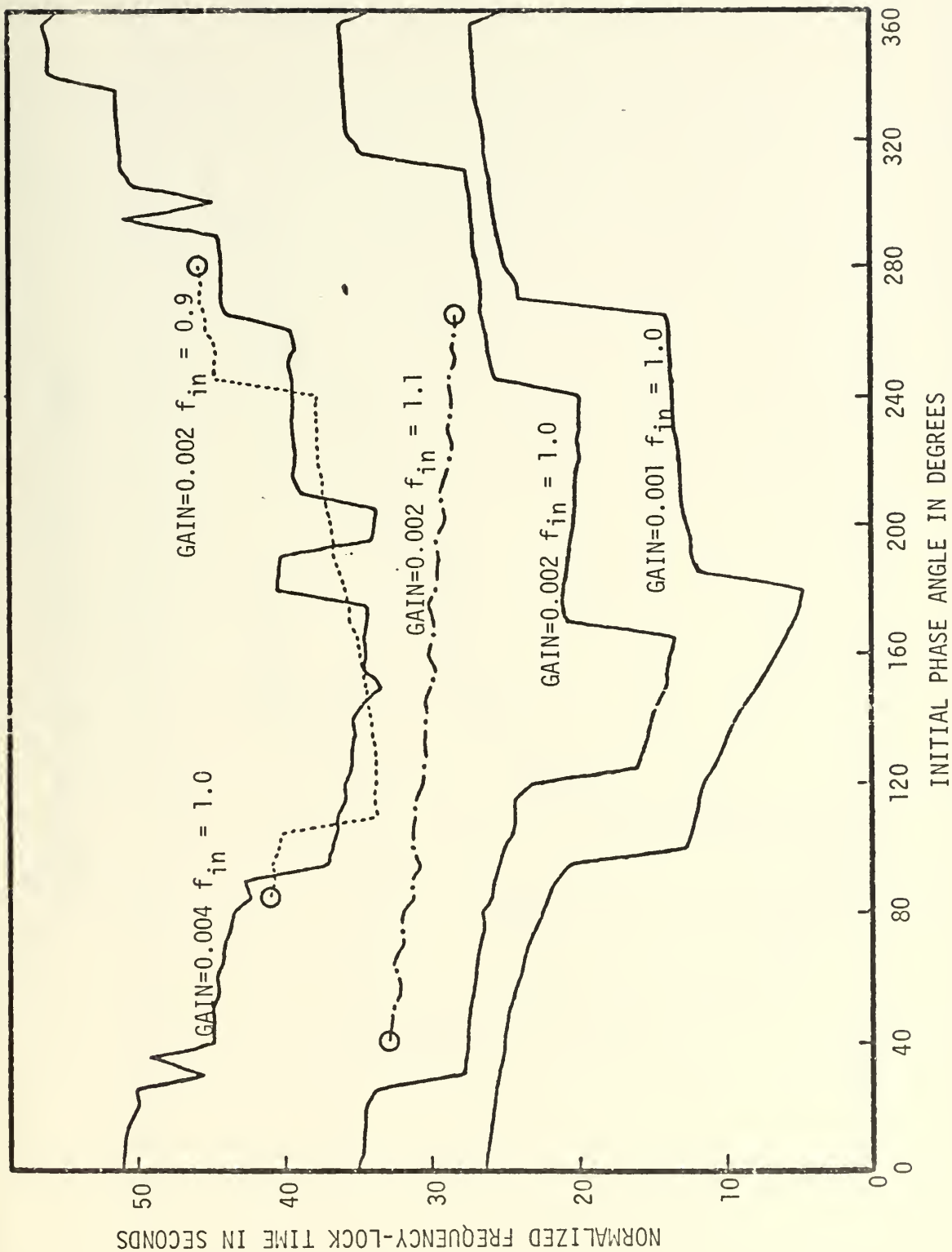


Figure V-G-2. Frequency-Lock Time as a Function of Initial Phase Angle for the Additive Phase Comparator with Track and Hold for Various Values of Gain and Input Frequencies as Specified on Each Curve.

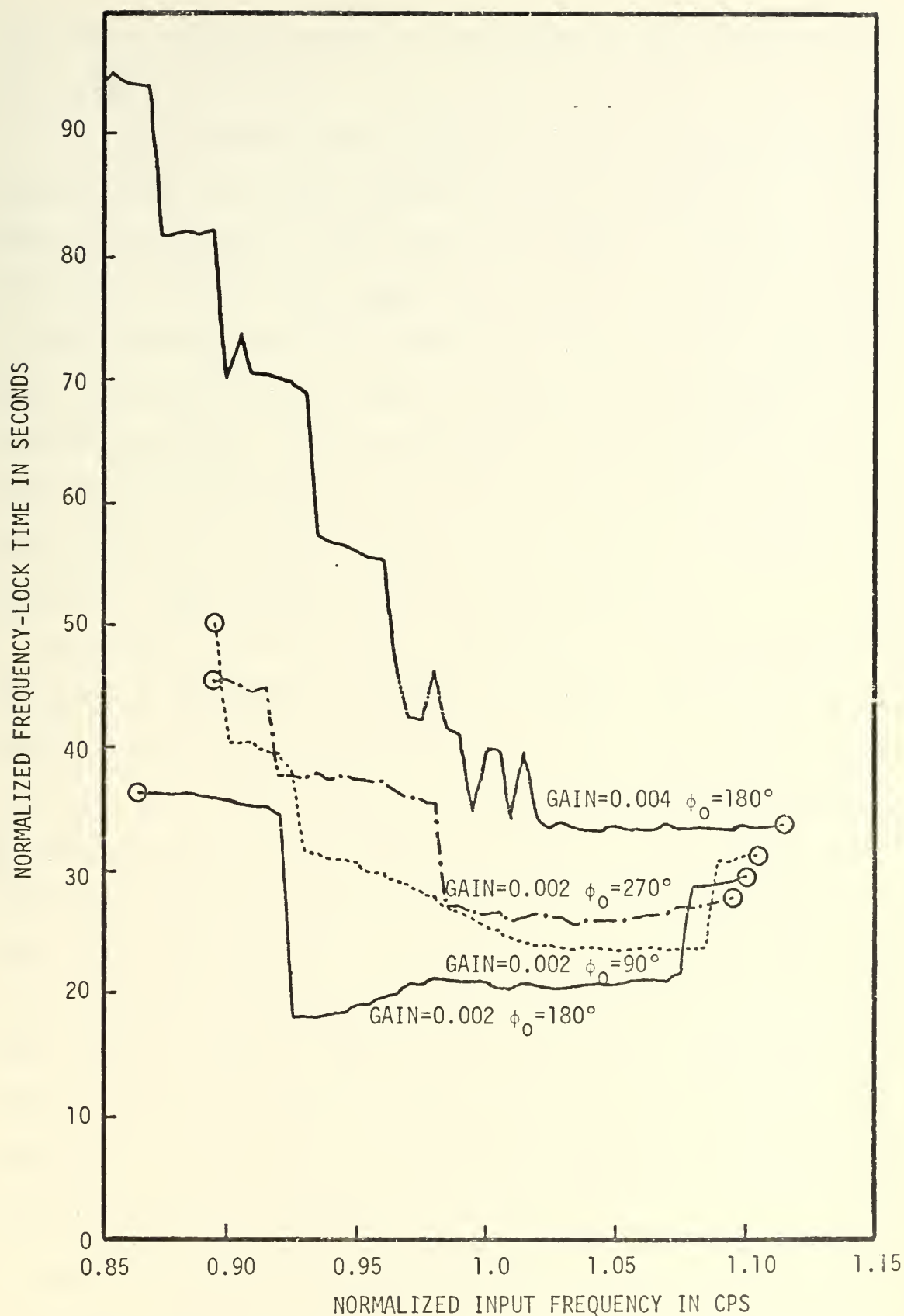


Figure V-G-3. Frequency-Lock Time as a Function of Input Frequency for the Additive Phase Comparator with Track and Hold for Various Values of Gain and Initial Phase as Specified on Each Curve.

reduction in the seize frequency of the system due to the addition of the track and hold circuit.

It is seen that the curve in Figure V-G-2 for a frequency of 0.9 cps displays greater lock times than the curve for a frequency of 1.1 cps, which is consistent with theory since it was shown in Subsection V, F that for the additive phase comparator the gain is increased for decreases in input frequency, and it has already been observed in this subsection that for the track and hold circuit an increase in gain results in increased lock time. This same relationship between frequency, gain, and lock time is displayed from a different point of view in Figure V-G-3, where again it is seen that increased lock times result from both decreases in input frequency and increases in system gain.

The effects of sampling on the stability of the additive phase comparator circuit have been demonstrated and have been found to be similar to the effects of sampling on the R-S phase comparator. However, while with the R-S phase comparator there had been some advantages gained by adding the track and hold circuit in regards to instantaneous VCO frequency variation and the ability of the circuit to operate with no input signal, these factors were not advantages here since the additive phase comparator already possessed these characteristics. The reduced seize frequency, reduced stability, and increased lock times together with the lack of any particular advantages serve to discourage the addition of a track and hold circuit to the additive phase comparator for phase-locked loop applications.

H. ADDITIVE NONLINEAR PHASE COMPARATOR

It has been determined previously in this treatise that the operation of the R-S phase comparator could be significantly improved by properly

inserting a nonlinearity in the phase comparator's characteristics, so that a greater corrective action would be generated when a large phase error existed. This same technique was also applied to the additive phase comparator, and two different forms of nonlinearity will be presented here, together with curves showing the resulting operating characteristics of each.

The first type of nonlinearity used with the additive phase comparator shall be called the exponential nonlinearity because of the way in which the output waveforms are generated. The operation of this additive exponential nonlinear phase comparator is shown in Figure V-H-1, and the circuit operation is identical with that depicted in Figure V-F-1 except that now the flip-flop outputs start at an initial voltage of \pm AMP and

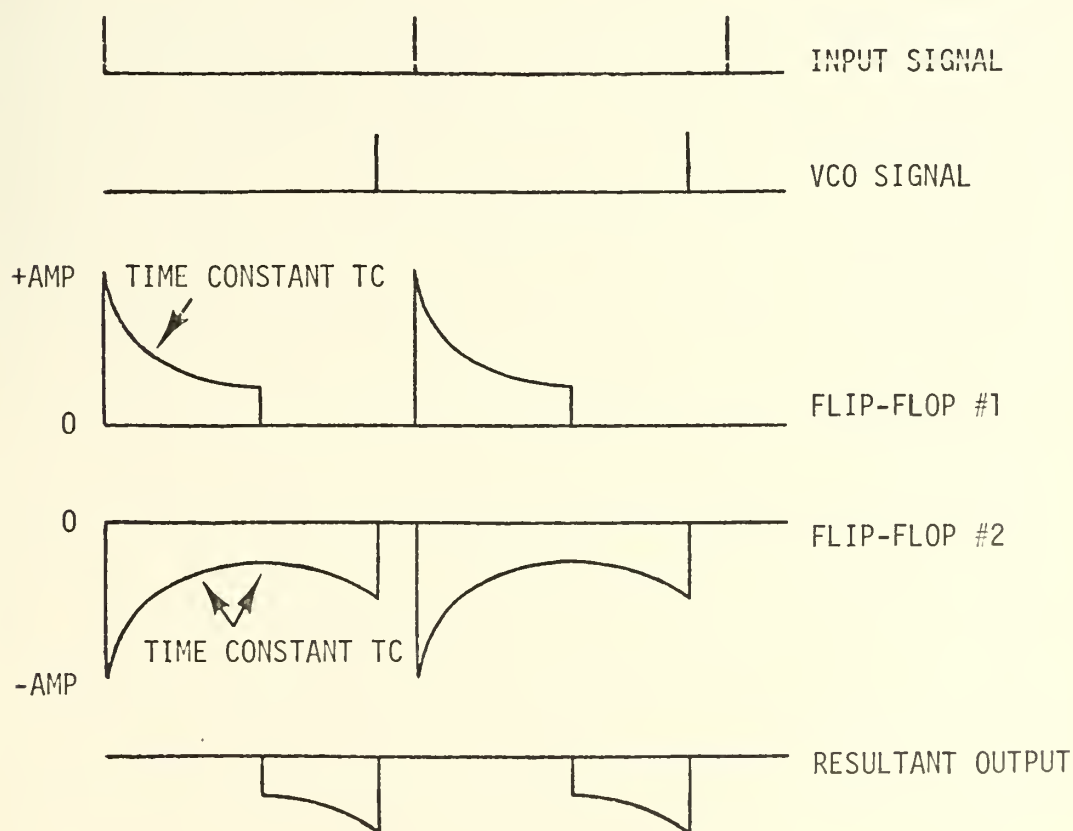


Figure V-H-1. Operation of the Additive Phase Comparator with the Exponential Nonlinearity.

vary exponentially as a function of time. The equation for the output voltage of flip-flop number one as a function of time with a normalized VCO center frequency of 1.0 cps is given by

$$V_{FF1} = \begin{cases} \text{AMP } e^{-TCt} & 0 \leq t \leq 0.5 \\ 0 & 0.5 < t \end{cases}, \quad (V-h-1)$$

and the output of flip-flop number two is given by

$$V_{FF2} = \begin{cases} -\text{AMP } e^{-TCt} & 0 \leq t \leq 0.5 \\ -\text{AMP } e^{-\frac{TC}{2}} e^{+TC(t - 0.5)} & t > 0.5 \end{cases}. \quad (V-h-2)$$

The waveforms shown in Figure V-H-1 are no longer simple pulses, and while the output of flip-flop number one can be generated with the use of an RC circuit similar to the procedure used for the R-S nonlinear phase comparator shown in Figure V-B-3, the waveform required at the output of flip-flop number two requires additional circuitry. The exponential output voltage of flip-flop number two can be generated by using several operational amplifiers connected as shown in Figure V-H-2. The switch S1 is initially closed, and the circuit operation is initiated by the arrival of each input pulse which causes the output voltage to start with an initial magnitude of -AMP and decay exponentially with a time constant TC. At a time which corresponds to one half the period of the VCO free running frequency the switch S1 is closed, and now the output voltage begins at its current value and increases exponentially in magnitude at the rate e^{TCt} . Therefore, although additional circuitry is required, the desired waveforms for the exponential nonlinearity can be generated without excessive complications, and if integrated circuit operational amplifiers were used the requirements of space and cost would not be excessive. The outputs of the two flip-flops are then added together to get the resultant output voltage as was done with the normal additive phase comparator. The

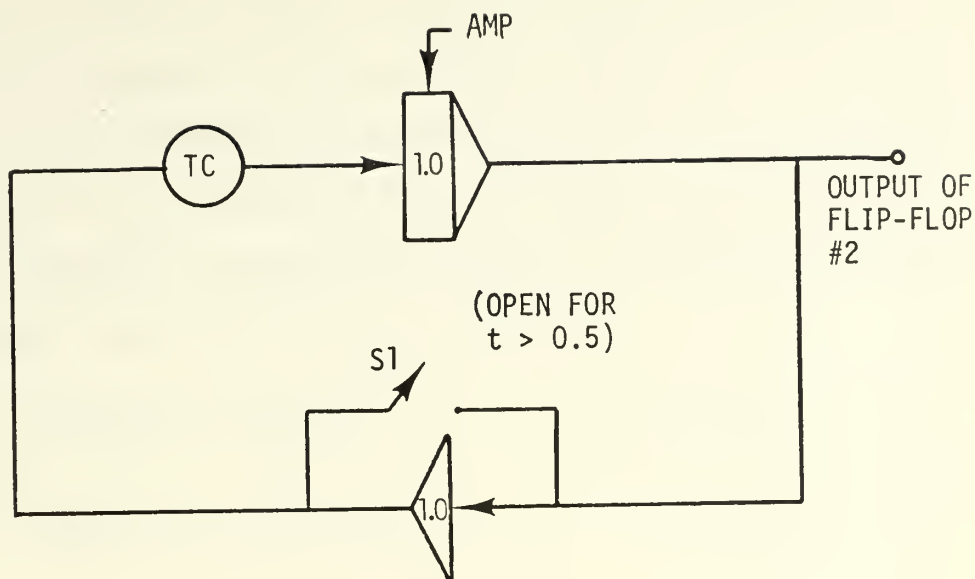


Figure V-H-2. A Method of Generating the Output Waveform of Flip-Flop Number Two for the Additive Phase Comparator with Exponential Nonlinearity.

general equation for the average output of the phase comparator as a function of the normalized input phase ϕ_{on} for a normalized VCO center frequency of 1.0 cps and for any value of the input signal period PD is given as

$$f(\phi_{on}) = \begin{cases} \int_0^{0.5} AMP e^{-TCt} dt + \int_0^{t_1} -AMP e^{-TCt} dt & 0 \leq t_1 \leq 0.5 \\ \int_{0.5}^{t_1} -AMP e^{-\frac{TC}{2}} e^{+TC(t - 0.5)} dt & t_1 > 0.5 \end{cases} \quad (V-h-3)$$

where t_1 is the time of arrival of the VCO pulse and is equal to $\phi_{on} PD$.

Equation V-h-3 can be integrated to yield

$$f(\phi_{on}) = \begin{cases} \frac{AMP}{TC} \left(-e^{-\frac{TC}{2}} + e^{-TC\phi_{on} PD} \right) & 0 \leq t_1 \leq 0.5 \\ \frac{AMP}{TC} e^{-TC} \left(-e^{TC\phi_{on} PD} + e^{\frac{TC}{2}} \right) & t_1 > 0.5 \end{cases} \quad (V-h-4)$$

In order to establish the relationship between AMP and TC which is required if the exponential nonlinear phase comparator is to have the same small signal operating characteristics as the normal additive phase comparator, it will be necessary to first determine the gain of the additive exponential nonlinear phase comparator. The general expression for this gain is given as

$$\frac{df(\phi_{on})}{d\phi_{on}} = \begin{cases} -(AMP)(PD) e^{-TC\phi_{on}} PD & 0 \leq t_1 \leq 0.5 \\ -(AMP)(PD) e^{TC(-1 + \phi_{on}) PD} & t_1 > 0.5 \end{cases} \quad (V-h-5)$$

Under the conditions where ϕ_{on} equals 0.5 and PD equals 1.0, which corresponds to steady state operating conditions for an input frequency of 1.0 cps, it was desired to have the gain of Equation V-h-5 equal to that of the normal additive phase comparator. It has been determined in Subsection V, f that the gain of the normal additive phase comparator was -1.0. Therefore an additional gain factor of -2.0 was obtained in the loop amplifier to make the overall gain correspond to +2.0 thus agreeing with both Equation III-a-13 and with the gain of the system using the R-S phase comparator. If the gain of Equation V-h-5 is set equal to -2.0 for the operating conditions specified above it is possible to express the magnitude of AMP as

$$AMP = 2.0 e^{+\frac{TC}{2}} \quad (V-h-6)$$

Throughout this work Equation V-h-6 will always be satisfied so that the small signal gain of the additive exponential nonlinear phase comparator is the same as that of the normal additive phase comparator, and therefore the value of the time constant TC will be the only variable used to adjust the degree of the nonlinearity.

A plot of the nonlinear phase comparator output as a function of the normalized phase angle for various values of TC and an input frequency of 1.0 cps is given in Figure V-H-3, together with the curve for the normal additive phase comparator output including the gain factor of -2.0. From this figure it is seen that the output characteristics in the vicinity of steady state are the same for both the normal and nonlinear curves, but that the nonlinear curves do develop a much greater corrective voltage as the phase error increases. The curves of Figure V-H-3 are very similar to those shown in Figure V-B-2 for the R-S nonlinear phase comparator except that for any given value of ϕ_{on} and TC the value of $f(\phi_{on})$ is greater for the additive exponential nonlinear curves than for the R-S nonlinear curves. Therefore, it is not necessary to use as large a value of TC for the additive as for the R-S nonlinear phase comparator.

When the system gain given in Equation V-h-5 is plotted as a function of input frequency with TC equal to 3.0 and for various values of the normalized input phase angle ϕ_{on} , the results are as shown in Figure V-H-4. The curves shown in Figure V-H-4 indicate that for large values of phase the system gain becomes extremely large at low values of input frequency. A similar phenomenon was observed in Figure V-B-10 for the R-S nonlinear phase comparator, but the variation of gain with frequency was not as great due to the fact that the voltage being developed at the output of the R-S phase comparator was decreasing exponentially with time, while for the additive phase comparator the output of flip-flop number two increases exponentially with time starting 0.5 seconds after the input pulse. Therefore, for low input frequencies where the period of time between input pulses becomes longer, the exponentially increasing voltage

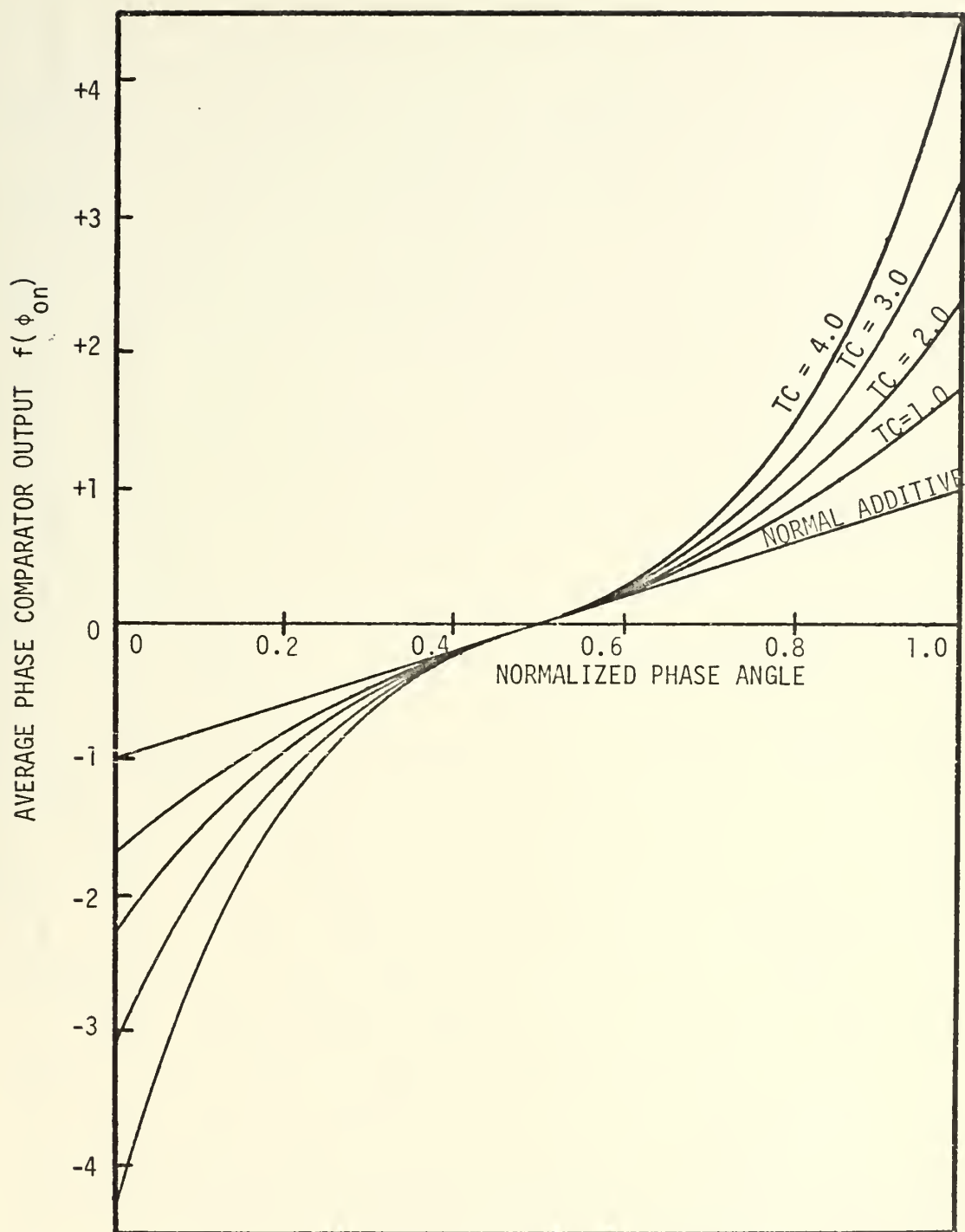


Figure V-H-3. Average Phase Comparator Output as a Function of the Normalized Phase Angle for the Additive Phase Comparator with Exponential Nonlinearity for Various Values of the Time Constant Together with the Curve for the Normal Additive Phase Comparator.

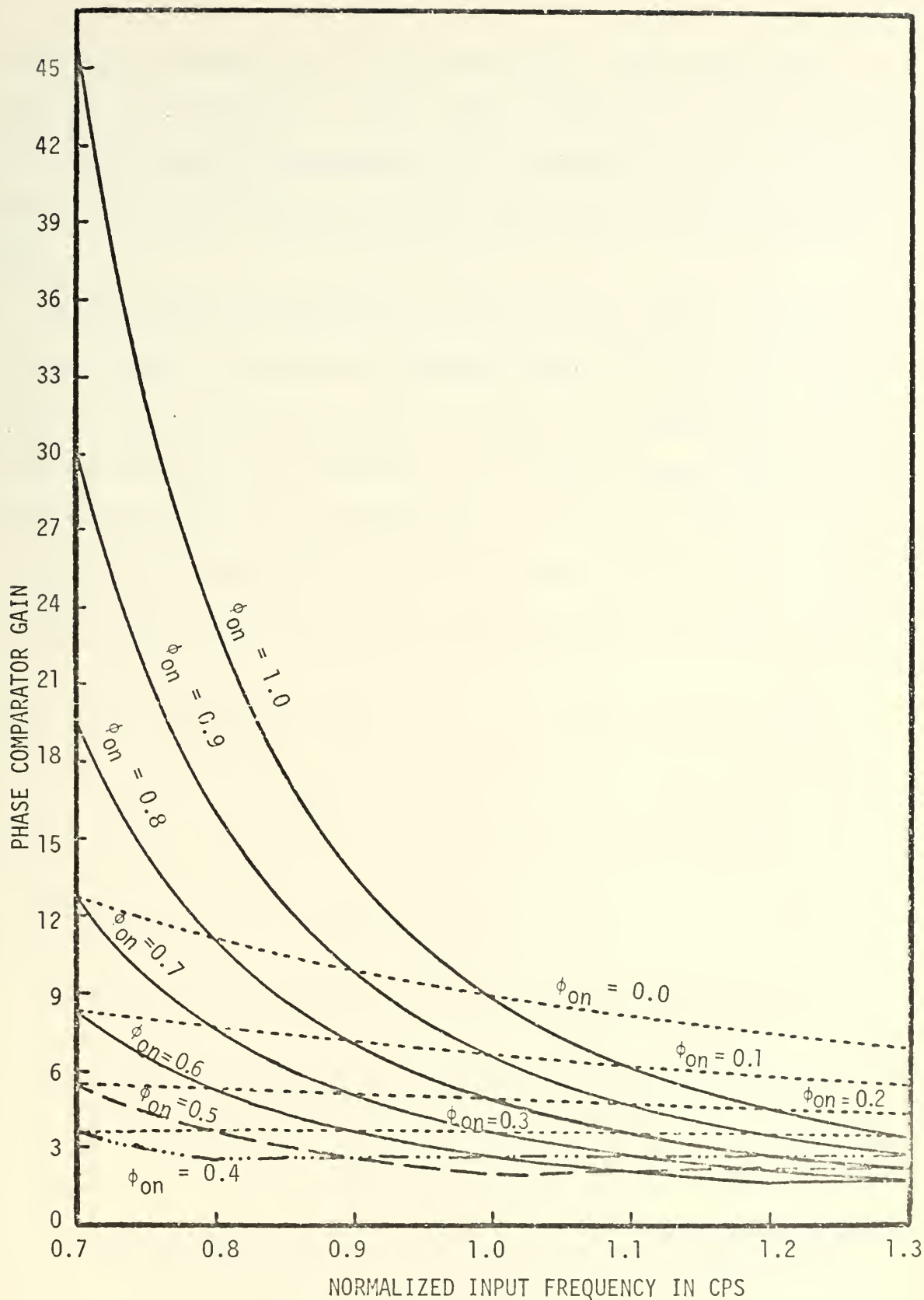


Figure V-H-4. Phase Comparator Gain as a Function of Frequency for the Additive Phase Comparator with an Exponential Nonlinearity and a Time Constant of 3.0.

causes the nonlinear gain to increase rapidly. For values of TC greater than that shown in Figure V-H-4, the gain at low frequencies and large phase angles increases even more drastically, becoming larger by a factor of several hundred times the normal additive phase comparator gain.

A second type of modification to the additive phase comparator circuit which also produces an increased output with increased phase error will now be presented, and this form will be referred to as the ramp nonlinearity. The operation of the additive phase comparator with ramp nonlinearity can be described with the help of Figure V-H-5 where H is the initial magnitude of the waveforms and α is the rate of change of voltage with time. It can be seen that the only essential difference

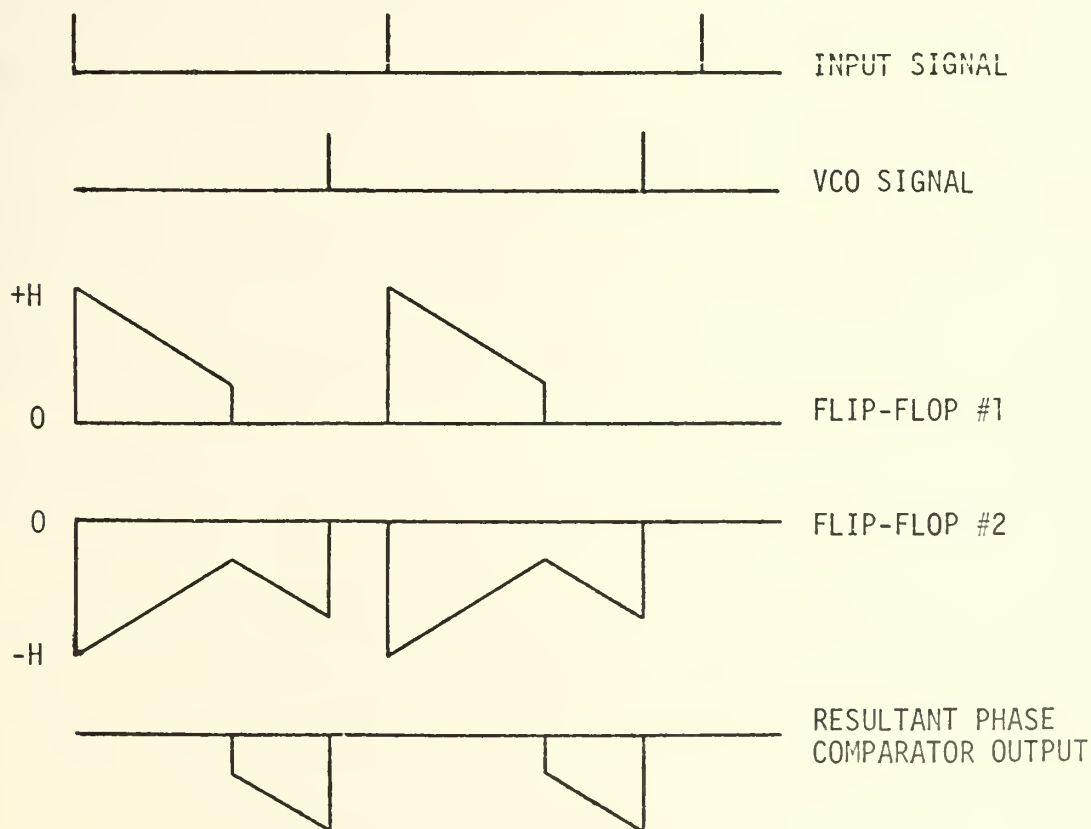


Figure V-H-5. Operation of the Additive Phase Comparator with the Ramp Nonlinearity.

between the ramp circuit shown in Figure V-H-5 and the exponential circuit shown in Figure V-H-1 is that in the ramp circuit the flip-flop output voltages change linearly with a slope α instead of exponentially. The ramp voltages can easily be generated by using operational amplifiers configured as integrators together with appropriate switching mechanisms.

The general equation for the average output of the ramp nonlinear phase comparator as a function of both phase and input frequency is given as

$$f(\phi_{on}) = \begin{cases} \int_0^{0.5} (H - \alpha x) dx - \int_0^{t_1} (H - \alpha x) dx & 0 \leq t_1 \leq 0.5 \\ \int_{0.5}^{t_1} [(-H + 0.5\alpha) - \alpha(x - 0.5)] dx & t_1 > 0.5 \end{cases} \quad (V-h-7)$$

which can be reduced to

$$f(\phi_{on}) = \begin{cases} 0.5H - 0.125\alpha - H\phi_{on} PD + 0.5\alpha\phi_{on}^2 PD^2 & 0 \leq t_1 \leq 0.5 \\ 0.5H - 0.357\alpha - (H - \alpha)\phi_{on} PD - 0.5\alpha PD^2 \phi_{on}^2 & t_1 > 0.5. \end{cases} \quad (V-h-8)$$

The general expression for the system gain is

$$\frac{df(\phi_{on})}{d\phi_{on}} = \begin{cases} -HPD + \alpha PD^2 \phi_{on} & 0 \leq t_1 \leq 0.5 \\ -HPD + \alpha PD - \alpha PD^2 \phi_{on} & t_1 > 0.5 \end{cases} \quad (V-h-9)$$

Equation V-h-9 has two variable quantities, initial amplitude H and the slope α , and as with the other nonlinear circuits it is possible to determine the relationships between these two variables by using the fact that the steady state gain must equal that of the normal additive phase comparator. Substituting into Equation V-h-9 with ϕ_{on} equal to 0.5

and PD equal to 1.0 and equating the results to -2.0, the value of α can be computed in terms of H as

$$\alpha = -4.0 + 2H \quad . \quad (V-h-10)$$

The average output of the additive ramp nonlinear phase comparator for an input frequency of 1.0 cps can now be plotted as a function of the normalized phase angle ϕ_{on} , and this plot is shown in Figure V-H-6 together with the curve for the normal additive phase comparator. A comparison of the curves of Figure V-H-6 with the curves of $f(\phi_{on})$ for the exponential nonlinearity shown in Figure V-H-3 indicates that even though all the curves have the same slope for a ϕ_{on} of 0.5, the slope of $f(\phi_{on})$ for the ramp nonlinearity is greater than the slope of $f(\phi_{on})$ for the exponential nonlinearity for small variations of ϕ_{on} from its steady state value. For large variations of phase the slope of $f(\phi_{on})$ becomes greater for the exponential nonlinearity than for the ramp nonlinearity. Thus, for small variations in phase the gain of the ramp nonlinear phase comparator tends to be greater, while for large phase errors the gain of the exponential nonlinear phase comparator tends to be the larger.

When the gain of the ramp nonlinear phase comparator given in Equation V-h-9 is plotted as a function of input frequency with an H of 8.0 and for various values of the normalized phase angle while maintaining the relationship of Equation V-h-10, the results are as shown in Figure V-H-7. Figure V-H-7 indicates that the additive ramp nonlinear phase comparator is similar to both the nonlinear circuits discussed previously in that the gain increases for low frequencies and large phase angles, and this increase in gain is slightly greater than that of the R-S nonlinear phase comparator, but much less than that of the additive exponential circuit. The reason why the variation is less for the ramp

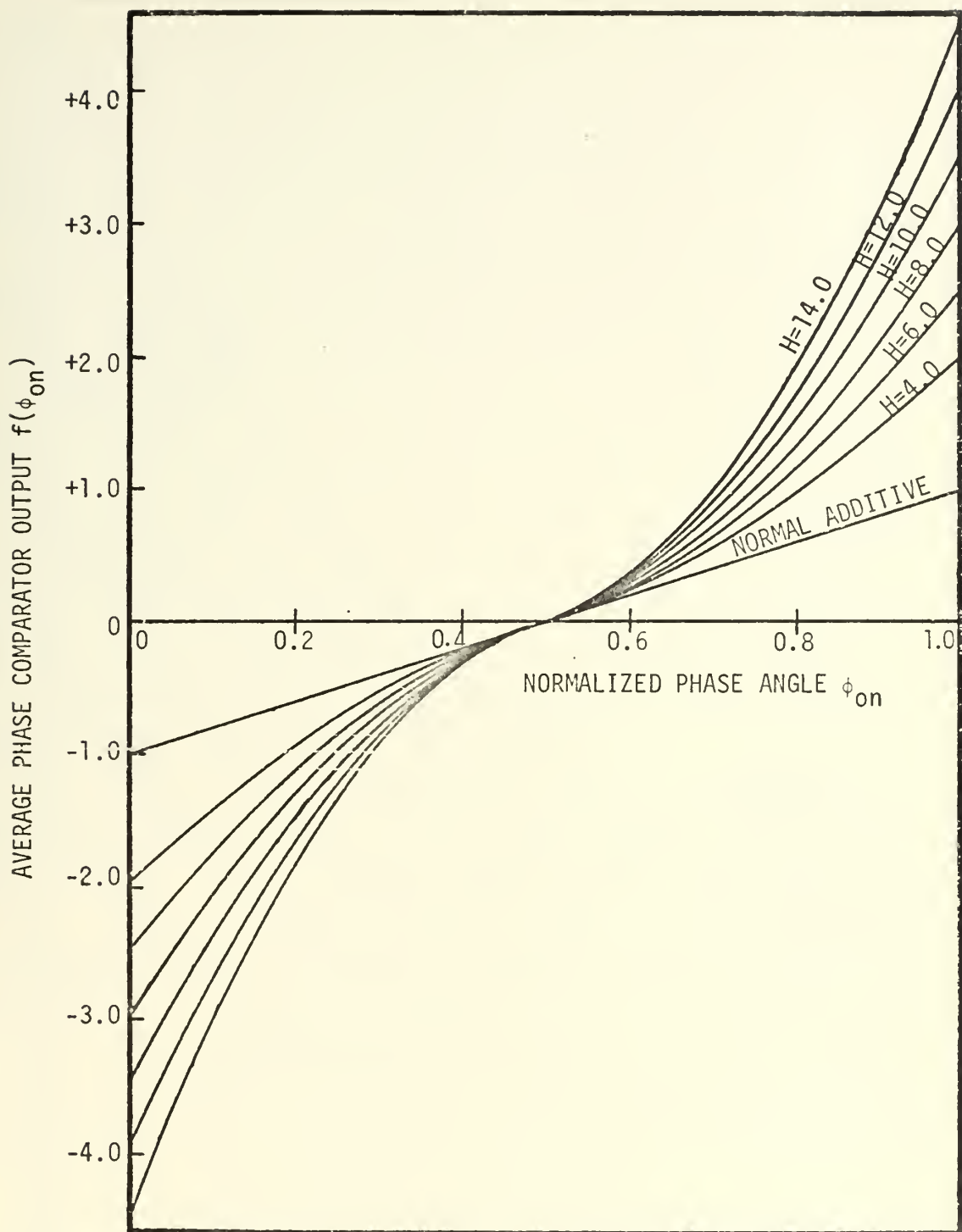


Figure V-H-6. Average Phase Comparator Output as a Function of the Normalized Phase Angle for the Additive Phase Comparator with a Ramp Nonlinearity and Various Values of the Amplitude H , together with the Curve for the Normal Additive Phase Comparator.

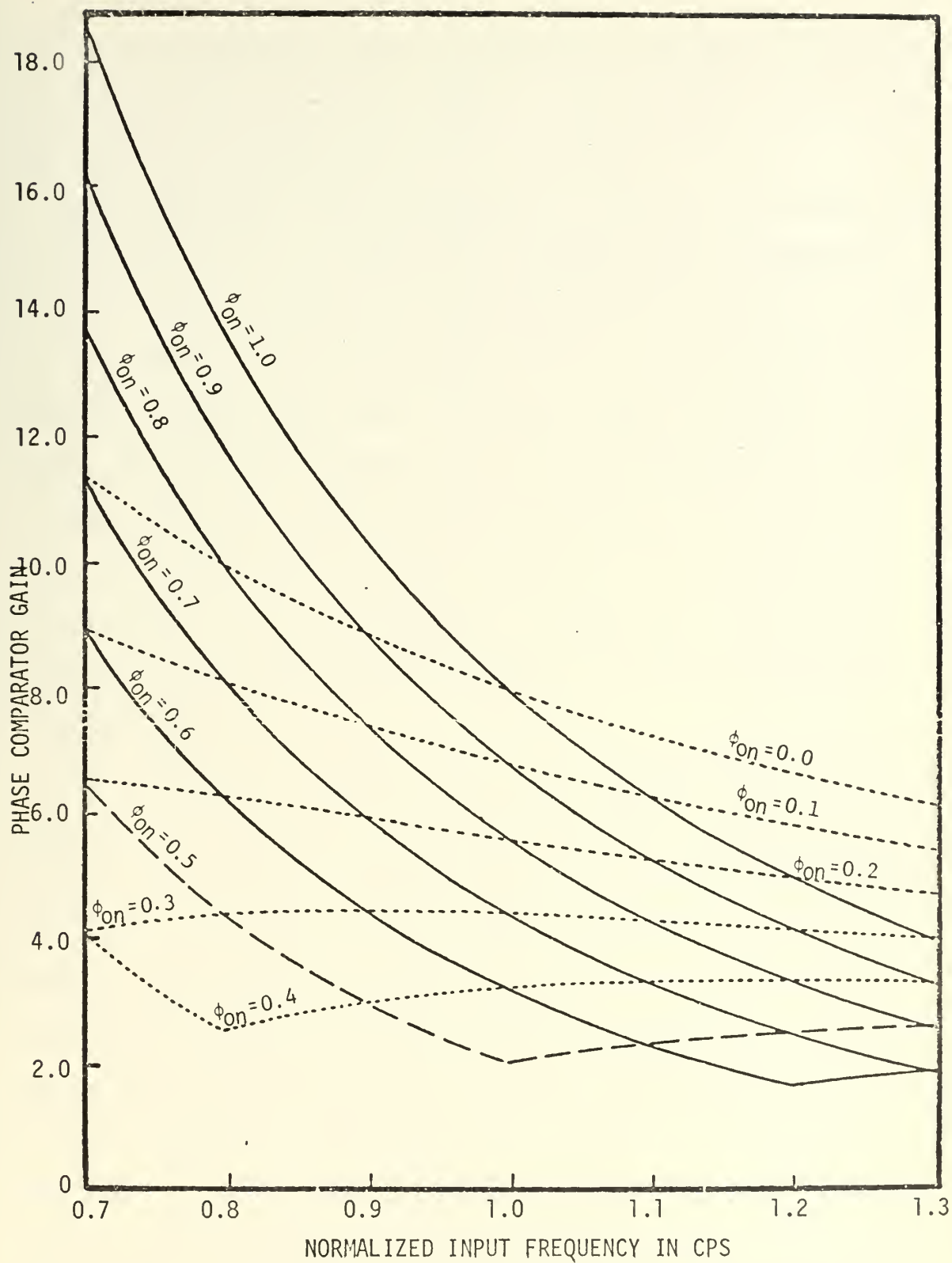


Figure V-H-7. Phase Comparator Gain as a Function of Frequency for the Additive Phase Comparator with a Ramp Nonlinearity with H of 8.0.

then for the exponential circuit is because with the ramp configuration the output voltage of flip-flop number two only increases linearly with time rather than exponentially.

Another phenomenon that can be observed in Figure V-H-7 is that some of the curves of gain as a function of frequency reach a minimum value and then start to increase again as evidenced in the curves for ϕ_{on} of 0.4, 0.5, and 0.6. This minimum gain point occurs when the VCO pulse coincides with the cutoff point of flip-flop number one shown in Figure V-H-5. When the input frequency is 1.0 cps then the VCO pulse occurs at the cutoff point for a normalized phase of 0.5, and for an input frequency of 1.2 and 0.8 the VCO pulse coincides with the cutoff of flip-flop number one for a ϕ_{on} of 0.6 and 0.4 respectively. These points mentioned above are the points which appear as minimums in the curves of Figure V-H-7.

The performance of the exponential phase comparator as a function of time is shown in Figure V-H-8 for a gain of 0.002, an input frequency of 1.1, an initial phase of 90 degrees, and for various values of the time constant TC. These curves are very similar to those for the R-S nonlinear phase comparator shown in Figure V-B-5, indicating that for these initial conditions the effect of the nonlinearity in the additive phase comparator is very similar to the effect of the nonlinearity on the R-S phase comparator. The effect of gain variations on the additive exponential nonlinear system is shown in Figure V-H-9 where the average frequency error is plotted as a function of time for the conditions of an input frequency of 1.1 cps, an initial phase of 90 degrees, and a time constant of 3.0. It can be seen that although the circuit becomes more oscillatory as the gain increases, no serious instability problems exist

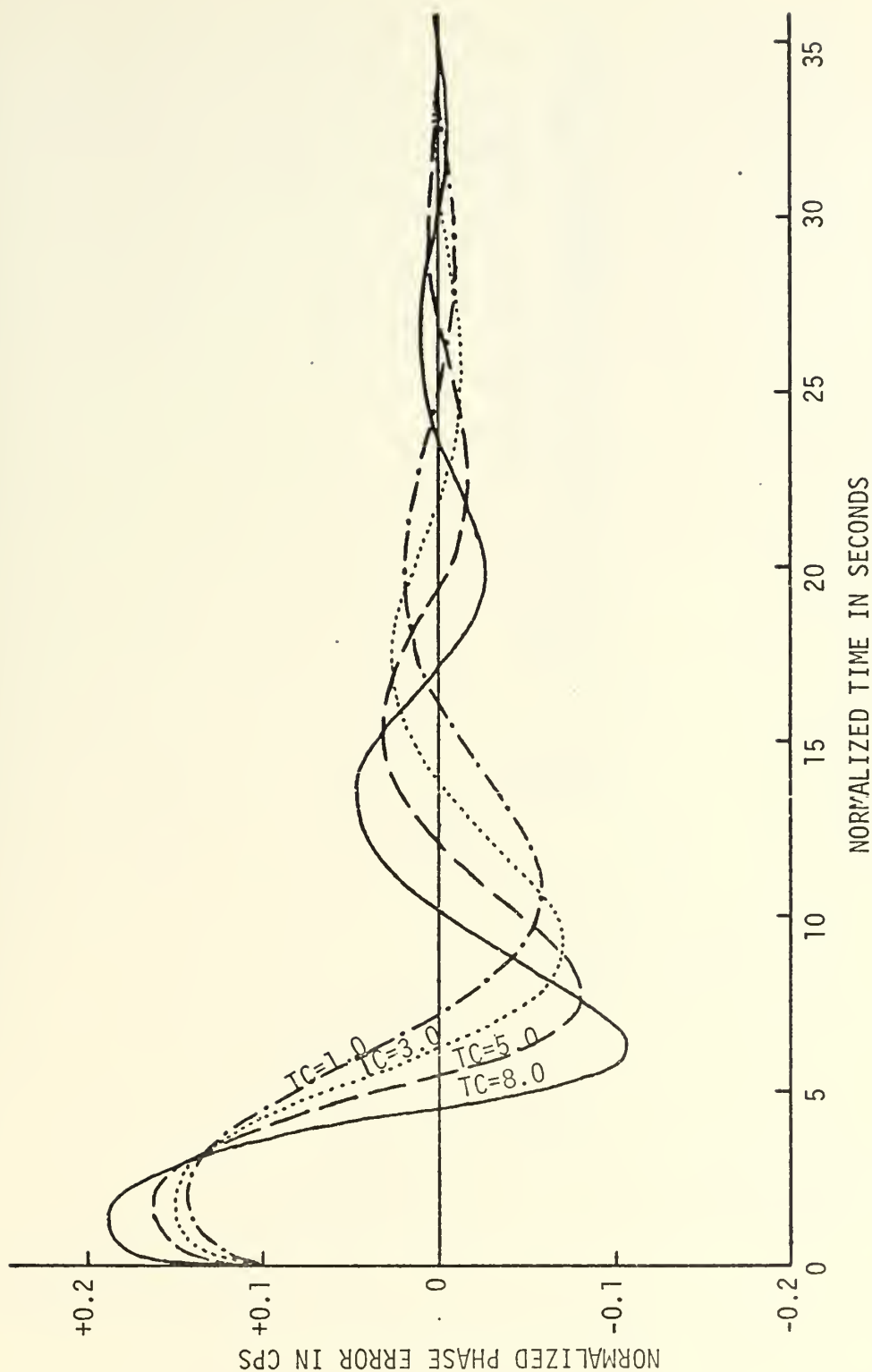


Figure V-H-8. Average Frequency Error as a Function of Time for the Additive Phase Comparator with Exponential Nonlinearity for an Input Frequency of 1.1 cps, Initial Phase of 90 Degrees, Gain of 0.002, and Various Values of the Time Constant.

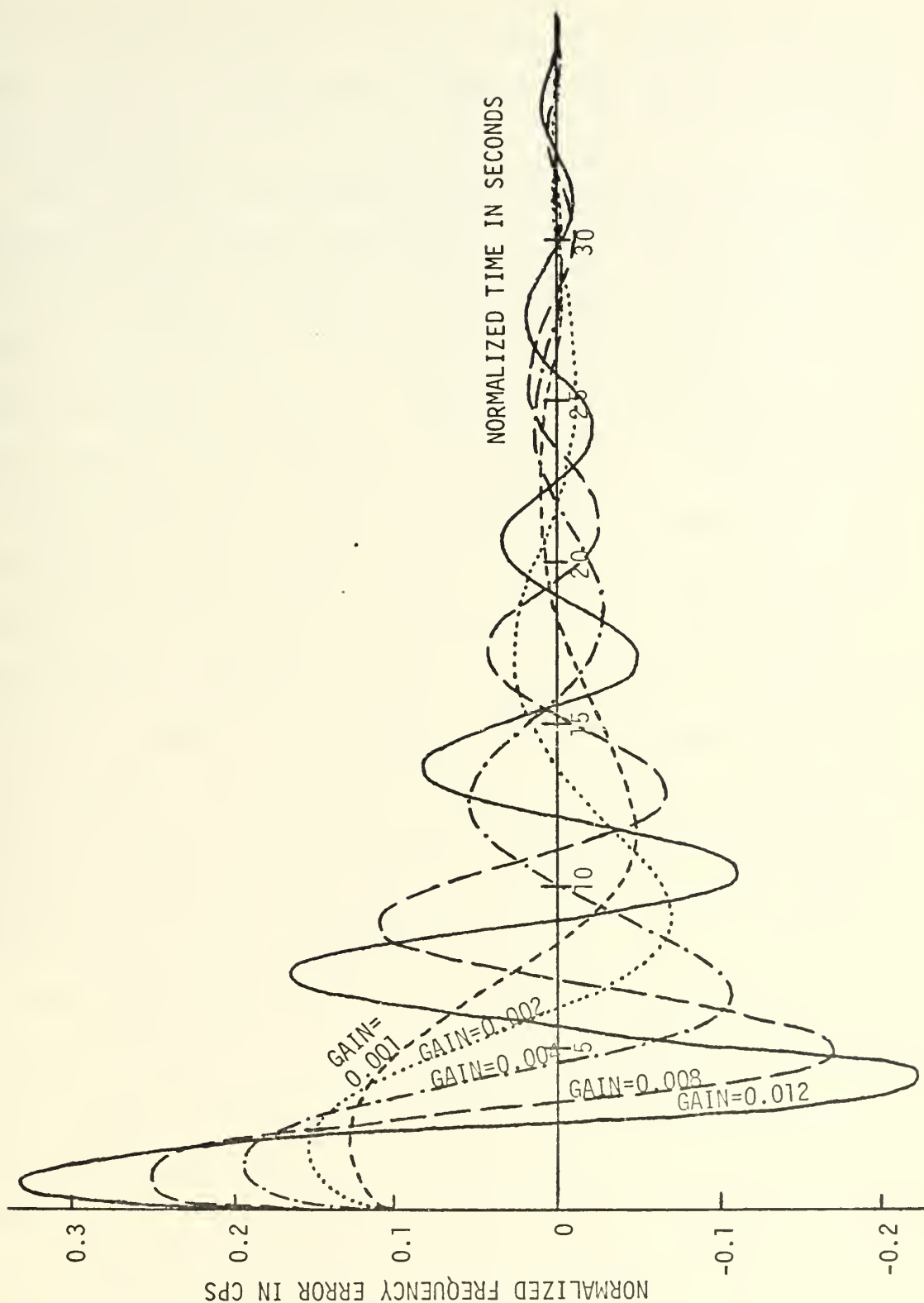


Figure V-H-9. Average Frequency Error as a Function of Time for the Additive Phase Comparator with Exponential Nonlinearity for an Input Frequency of 1.1 cps, Initial Phase of 90 Degrees, Time Constant of 3.0, and for Various Values of the Loop Gain.

for this particular set of initial conditions, and these curves also appear similar to those shown in Figure V-B-6 for the R-S nonlinear phase comparator.

The operation of the additive ramp nonlinear phase comparator exhibited some variations from that of both the additive exponential and the R-S nonlinear circuits. These differences can be seen from Figures V-H-10 and V-H-11 which show the average frequency error for the ramp nonlinear circuit as a function of time for variations in H and variations in gain respectively. Both families of curves shown in Figures V-H-10 and V-H-11 exhibit a much more oscillatory behavior as the system proceeds towards lock than did the other nonlinear systems studied. This increased oscillatory behavior is a result of the increased phase comparator output for small variations in phase as shown by the phase comparator characteristic curves of Figure V-H-6. Thus, even though the actual steady state gain is equal for all systems, the ramp nonlinearity has the highest gain for small phase errors in the vicinity of the steady state value, and therefore it takes a longer time for the system oscillations to damp out.

The system phase-lock time as a function of initial phase is shown plotted in Figure V-H-12 for the additive ramp nonlinear circuit with a gain of 0.002, initial amplitude H of 8.0, and for various values of the input frequency. The phase-lock time is seen to exhibit only a relatively small variation with phase for any given frequency, and this characteristic is similar to that observed for the R-S nonlinear phase comparator in Figure V-B-7. Thus, the increased gain with increased phase error has been effective in reducing the lock time for wide phase variations. It can also be observed that the lock times for an input frequency of 1.1

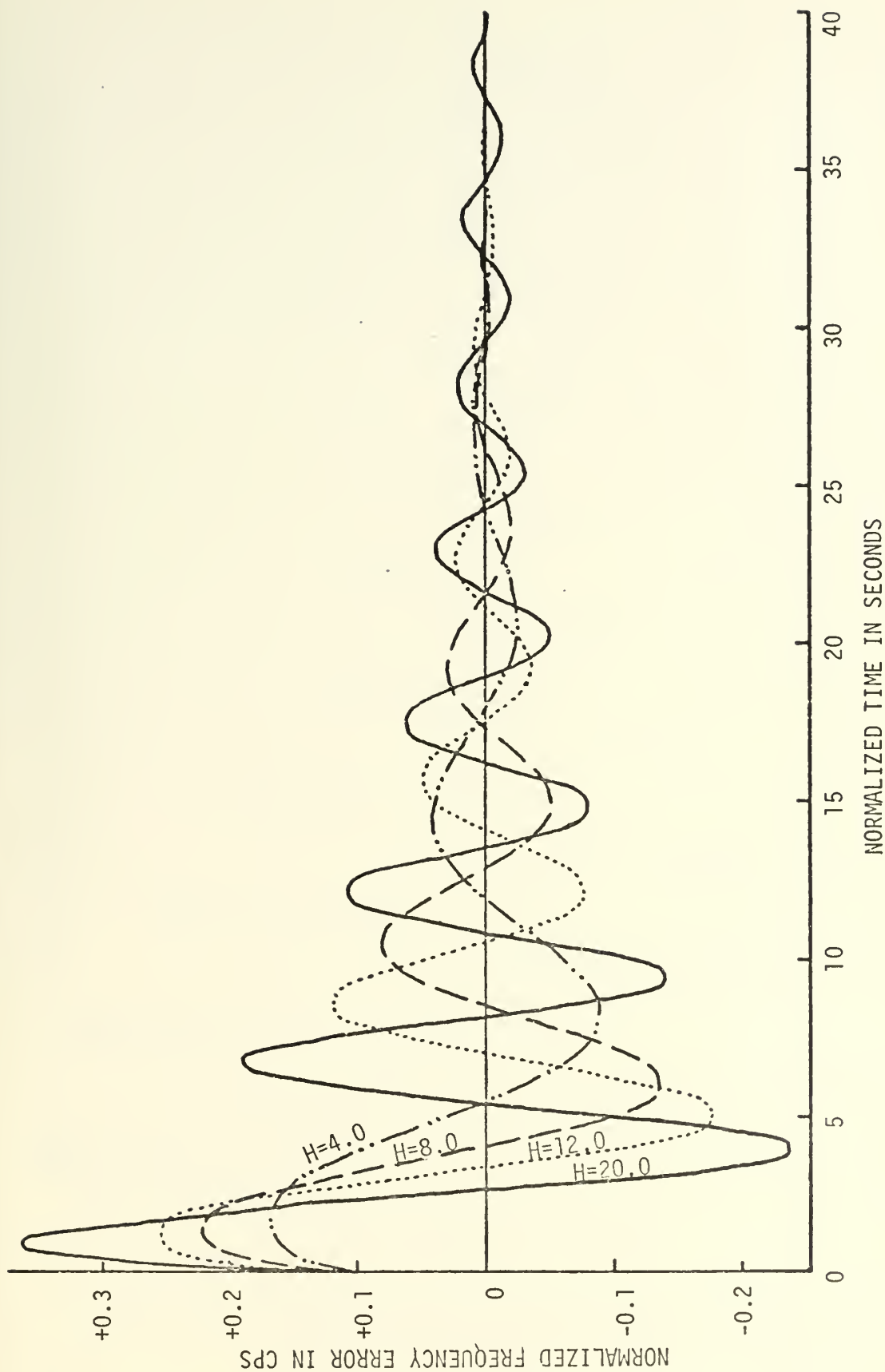


Figure V-H-10. Average Frequency Error as a Function of Time for the Additive Phase Comparator with Ramp Nonlinearity for an Input Frequency of 1.1 cps, Initial Phase of 90 Degrees, Gain of 0.002, and Various Values of the Amplitude H .

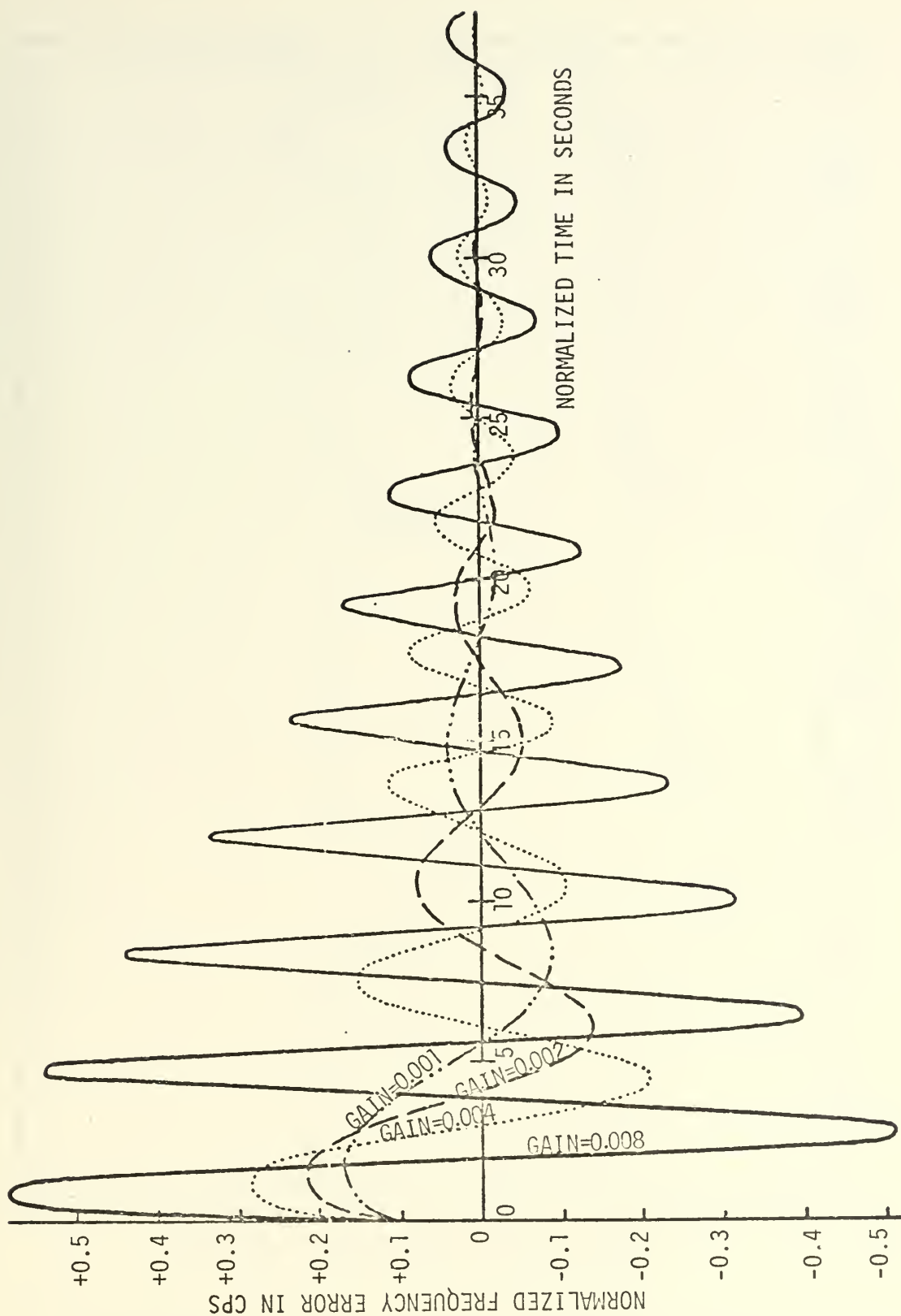


Figure V-H-11. Average Frequency Error as a Function of Time for the Additive Phase Comparator with Ramp Nonlinearity for an Input Frequency of 1.1 cps, Initial Phase of 90 Degrees, Initial Amplitude H of 8.0, and for Various Values of the System Gain.

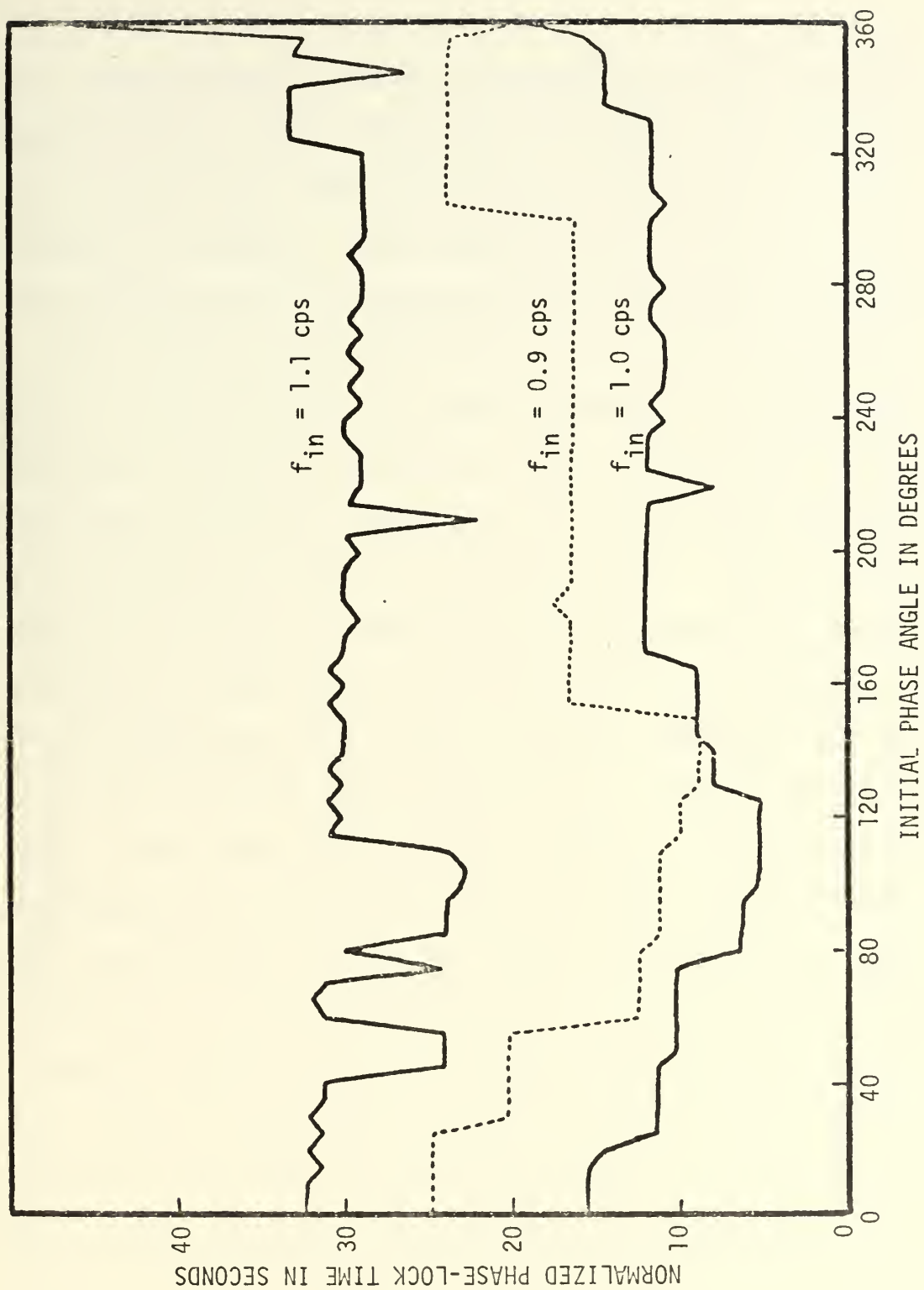


Figure V-H-12. Phase-Lock Time as a Function of Initial Phase for the Additive Phase Comparator with Ramp Nonlinearity with a Gain of 0.002 and an Initial Amplitude H of 8.0.

cps are significantly greater than those for an input frequency of 0.9 cps. This increased lock time for increased input frequency concurs with expected results since in the ramp nonlinear phase comparator characteristic curves shown in Figure V-H-7, the gain was seen to decrease for increases in frequency. These decreased lock times for low values of input frequency were also observed for the R-S nonlinear phase comparator.

The variation of frequency-lock times as a function of phase is shown in Figure V-H-13 for the additive exponential nonlinear phase comparator with a gain of 0.002 and a time constant of 5.0. This figure shows that for an input frequency of 1.0 cps the system frequency-lock time is also quite uniform as a function of phase, but for input frequencies either above or below the center VCO frequency the system performance is quite varied. For low values of input frequency the gain of the system varies over a very wide range as the phase angle changes, and as the gain varies certain combinations of gain and phase occur which result in very rapid frequency-lock. However, for other values of phase the system gain is either too large or too small to yield a rapid lock, and a longer time is required for the system to settle out. For an input frequency of 1.1 cps the frequency-lock time is uniform for low values of phase but becomes erratic for higher values of phase due to the reduced gain for large ϕ_{on} as shown in Figure V-H-4. In fact, the system even completely fails to lock for most large values of the normalized initial phase angle. This failure to lock for an input frequency of 1.1 cps and large values of initial phase has been observed in Figure V-F-6 for the normal additive phase comparator, but the range of phase over which the system would not lock is even greater for the exponential nonlinear than for the normal additive phase comparator. It must be noted that this characteristic of failing to lock for particular operating conditions was

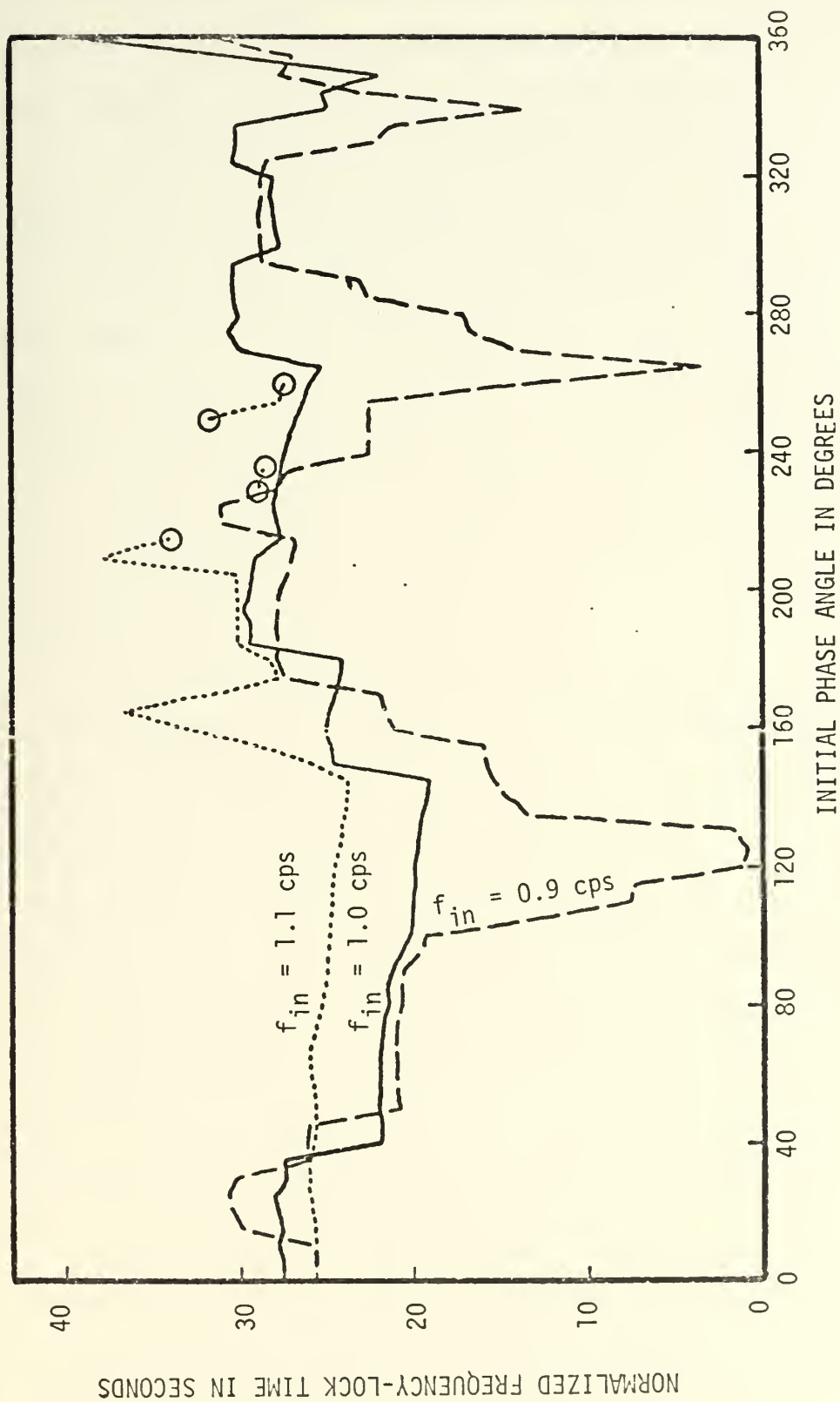


Figure V-H-13. Frequency-Lock Time as a Function of Initial Phase for the Additive Phase Comparator with Exponential Nonlinearity, a Gain of 0.002, and a Time Constant of 5.0.

not observed for the additive phase comparator with the ramp nonlinearity, since the ramp nonlinearity did not exhibit as great a variation of gain as a function of phase and therefore yielded less erratic operation.

One item not apparent from Figure V-H-13 but which could be obtained directly from the computer output was the fact that the maximum number of cycles that were skipped for the exponential nonlinear system with the system still being able to attain lock was four, and this number was found to occur in only one instance. The usual limit to the number of cycles that could be skipped and the system still attain lock was only one. In this respect the additive nonlinear phase comparator was very similar to the normal additive phase comparator and to the additive phase comparator with a ramp nonlinearity.

The system phase-lock performance as a function of frequency is shown in Figures V-H-14 and V-H-15 for the exponential and ramp nonlinear additive phase comparators respectively. These curves were made with both systems operating at a gain of 0.002, an H of 8.0 for the ramp nonlinearity, a TC of 5.0 for the exponential nonlinearity, and for various values of initial phase. For both families of curves it is seen that the lock times are greater and the lock ranges shorter for high values of input frequency than for low values, and this concurs with previous data for these circuits which indicates the presence of increased gain with decreased frequency. The ramp nonlinear phase comparator exhibited a flatter response over a wider range of frequencies than did the exponential nonlinear phase comparator. However, neither the curves of Figure V-H-14 nor Figure V-H-15 displayed any wide deviation of lock times for the various values of initial phase angle.

The operation of both the ramp and exponential nonlinear additive phase comparators for large frequency variations is shown in Figure V-H-16,

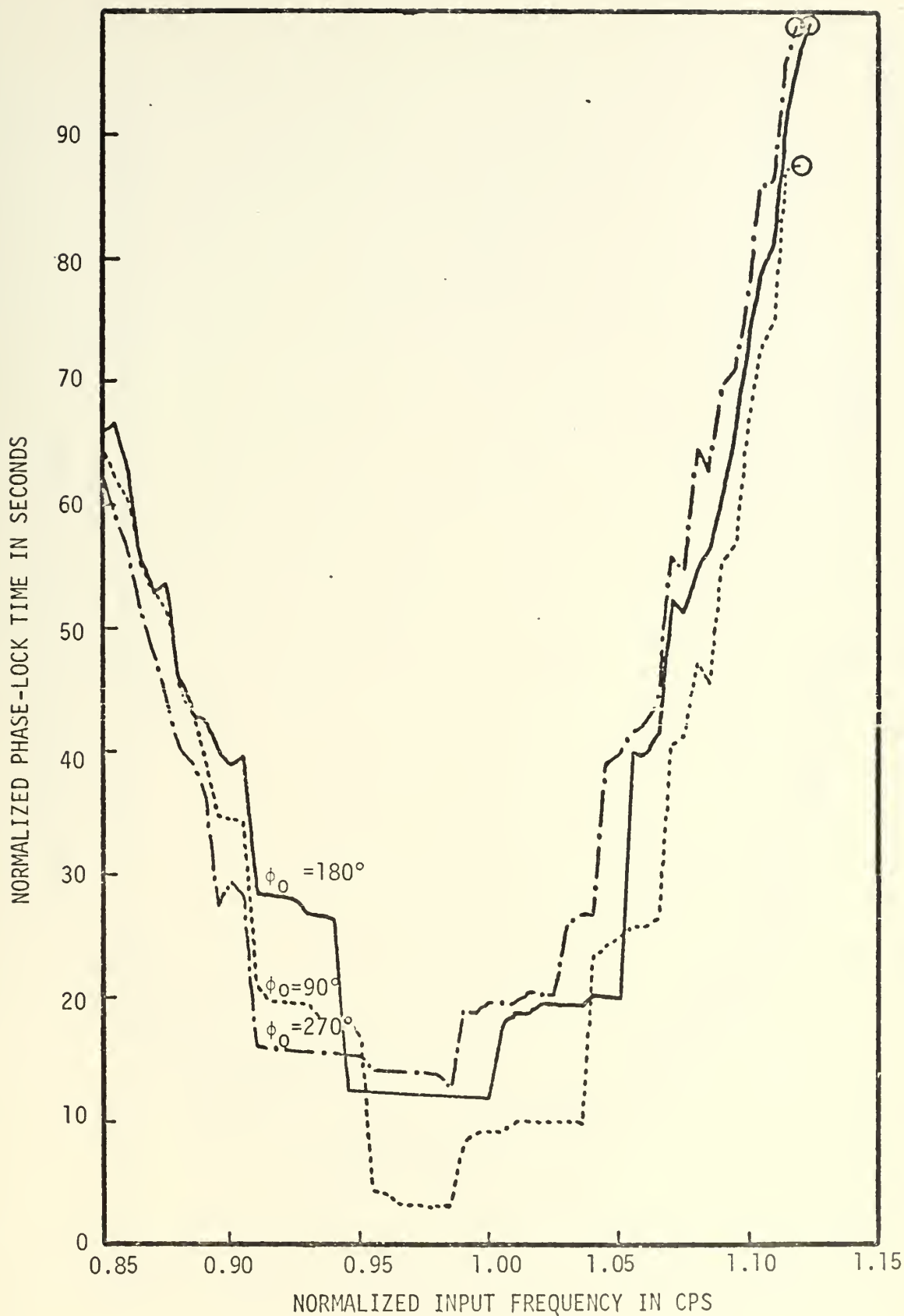


Figure V-H-14. Phase-Lock Time as a Function of Input Frequency for the Additive Phase Comparator with Exponential Nonlinearity for a Gain of 0.002 and a time Constant of 5.0.

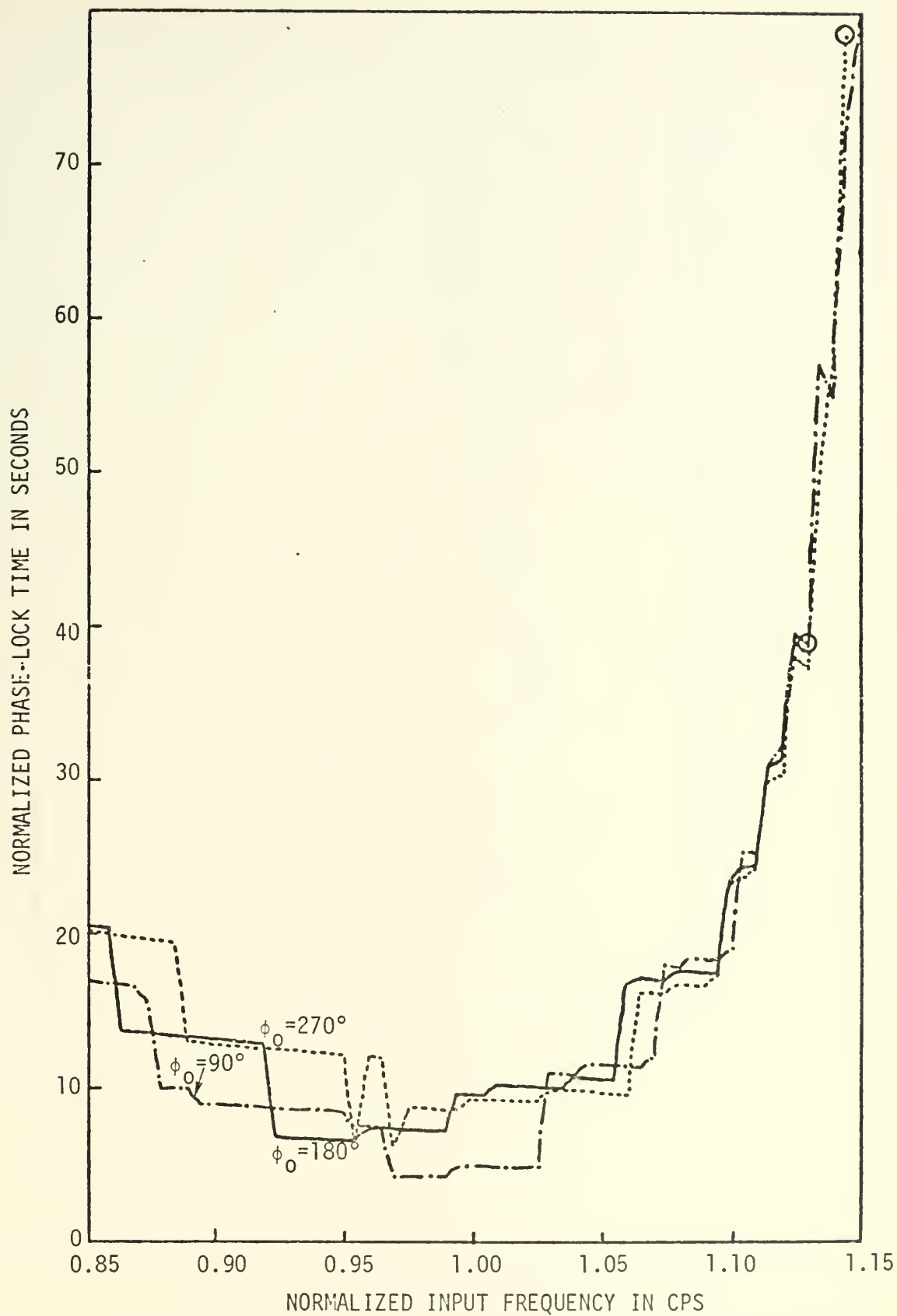


Figure V-H-15. Phase-Lock Time as a Function of Input Frequency for the Additive Phase Comparator with Ramp Nonlinearity, A Gain of 0.002, and an Initial Amplitude H of 8.0.

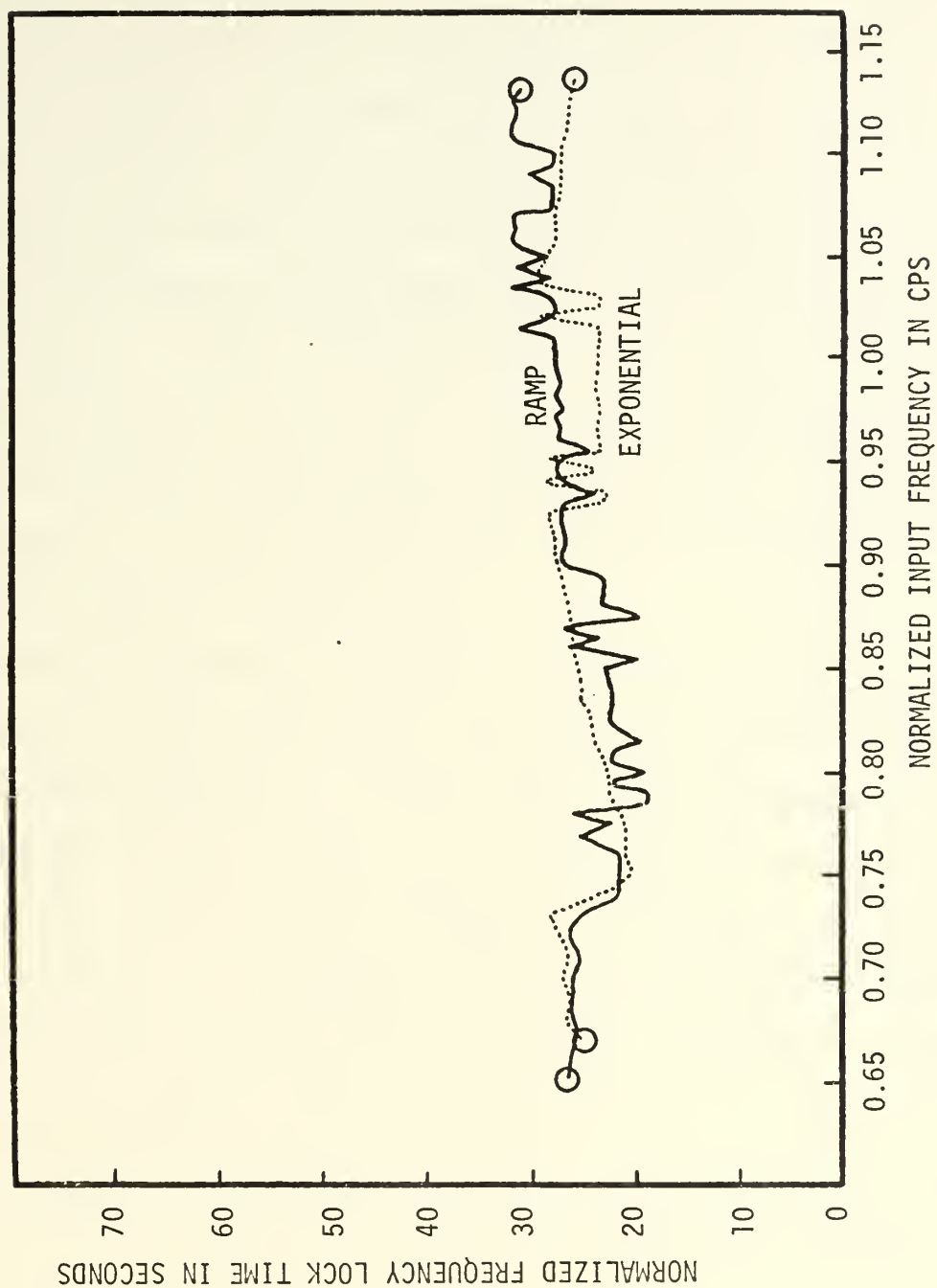


Figure V-H-16. Frequency-Lock Time as a Function of Input Frequency for the Additive Phase Comparator with both the Exponential and Ramp Nonlinearity for a Gain of 0.002, Initial Phase of 180 Degrees, $H = 8.0$ for the Ramp, and $TC = 5.0$ for the Exponential Nonlinearity.

where the frequency-lock time is shown as a function of the input frequency for an initial phase of 180 degrees, a gain of 0.002, TC of 5.0 for the exponential circuit, and H of 8.0 for the ramp circuit. It is seen that the lock range is very restricted for high values of input frequencies, but that the system will continue to lock even for exceptionally low values of input frequency due to the increased gain for low frequencies. For both of these particular curves no cycle skipping occurred, and even for the very low frequencies it was observed that once a single cycle was skipped the system would not lock. The performance in this respect is somewhat different from that seen in Figure V-H-13 where some cycle skipping was experienced.

The seize frequency as a function of phase for various values of the system gain and the initial flip-flop voltage H is shown in Figure V-H-17 for the ramp nonlinearity. A comparison of the seize frequency curves for the ramp nonlinearity with the curves of seize frequency for the normal additive system given in Figure V-F-7 indicates that the ramp nonlinear system has a significantly increased range of seize frequency over that of the normal additive phase comparator. Since the seize frequency is so closely correlated with the lock range for all forms of the additive phase comparator, the improved characteristics of the ramp nonlinearity shown in Figure V-H-17 also indicate an extended lock range over most values of the initial phase angle.

The curves of seize frequency versus phase for the exponential nonlinearity given in Figure V-H-18 do not indicate as good a system performance as those for the ramp nonlinearity given in Figure V-H-17. In fact, for all curves except those for low values of TC at low frequencies the system fails to function properly in that for large values of initial phase the rapid variations of the gain characteristics with

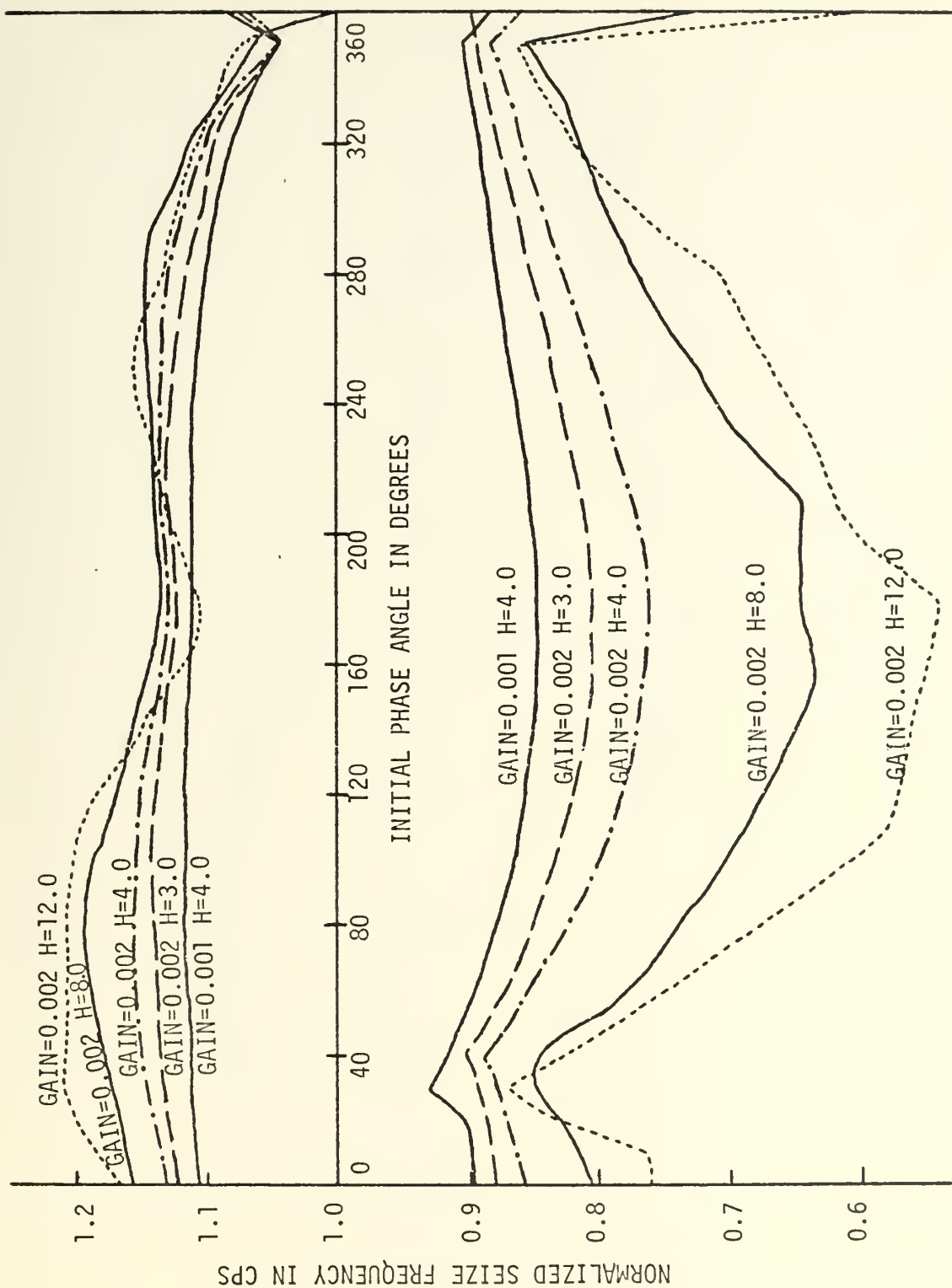


Figure V-H-17. Seize Frequency as a Function of Initial Phase for the Additive Phase Comparator with Ramp Nonlinearity.

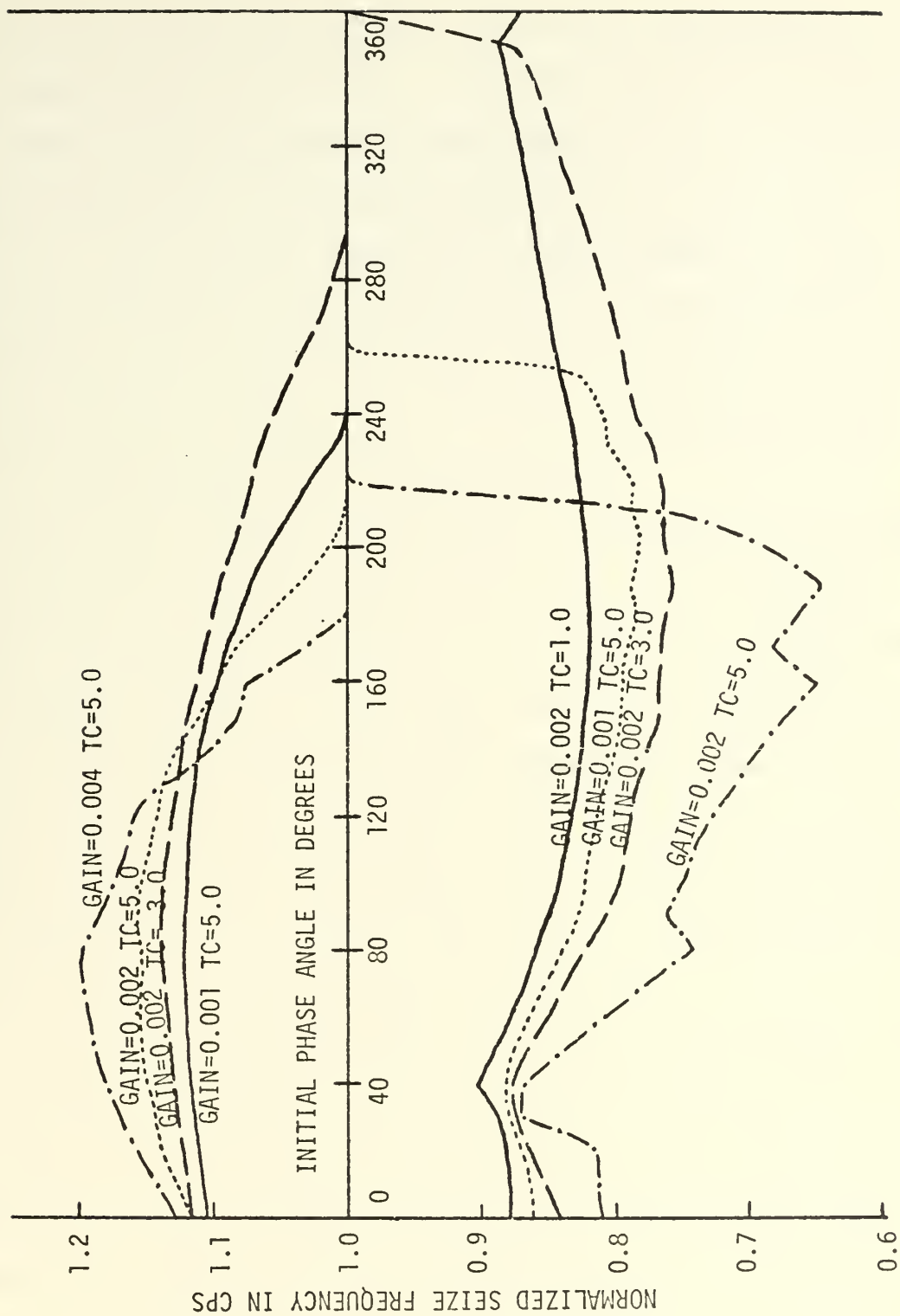


Figure V-H-18. Seize Frequency as a Function of Initial Phase for the Additive Phase Comparator with Exponential Nonlinearity.

frequency cause the system to fail to lock without cycle skipping. For high frequencies and large values of phase the gain is too low, and for low values of input frequency and large values of phase the system gain becomes so great that the system also fails to lock without cycle skipping. This is another example of the same phenomenon which was observed in Figure V-H-13 for large values of input phase and for an input frequency of 1.1 cps. This inability of the exponential circuit to function properly for large values of initial phase make the circuit appear undesirable for use in most applications.

In many other operating characteristics the nonlinear additive phase comparators closely resemble the basic additive circuit, and neither the ramp nor the exponential nonlinear circuit experiences any instantaneous VCO frequency variation in steady state. Both nonlinear additive circuits also have exactly the same steady state phase error as does the normal additive phase comparator and which is given by Equation V-f-4. This is because in steady state there can be no output from the phase comparator and therefore the VCO pulse must occur exactly at the point where the voltage output of flip-flop number one goes to zero.

It has been seen that the addition of certain nonlinearities to the additive phase comparator circuit can improve the system performance by yielding an increased seize frequency and an increased frequency lock range, together with reduced lock times over a wider range of input frequencies. However, care must be taken in selecting the form of the nonlinearity, and of the two systems investigated it was determined that the ramp nonlinearity exhibited a more satisfactory set of overall characteristics due to the less radical variations in system gain with frequency for large values of the system phase angle, although both

systems exhibited excellent performance for low values of the normalized initial phase angle.

I. SUMMARY OF PHASE COMPARATOR CHARACTERISTICS

In the preceding portions of this section the operating characteristics of a number of different phase comparators have been discussed in detail, and in this subsection a very brief summary will be presented to assist the reader in comparing the attributes of the various circuits. Since the results given both here and in all preceding work have been presented in terms of normalized values, the data provided can be used as a basis for design when selecting a phase comparator to meet the requirements of a particular application. The families of curves selected for presentation in this subsection were chosen because of their ability to give a precise overall representation of the various systems studied.

Several important operating characteristics are demonstrated for each phase comparator by the curves of frequency-lock time as a function of input frequency given in Figure V-I-1. These curves were all made for the identically same operating condition with a gain of 0.002 and an initial phase of 180 degrees, and therefore any variation in lock time with frequency occurs as a result of differences in each of the basic phase comparator's performance. One of the fundamental differences which influences the shape of the curves of Figure V-I-1 is the way in which the gain of each phase comparator varies as a function of frequency for the particular value of phase shown. This variation of gain with frequency results in some phase comparators exhibiting faster lock times for low than for high values of input frequency, while for other phase comparators the effect is reversed. For a detailed analysis of the

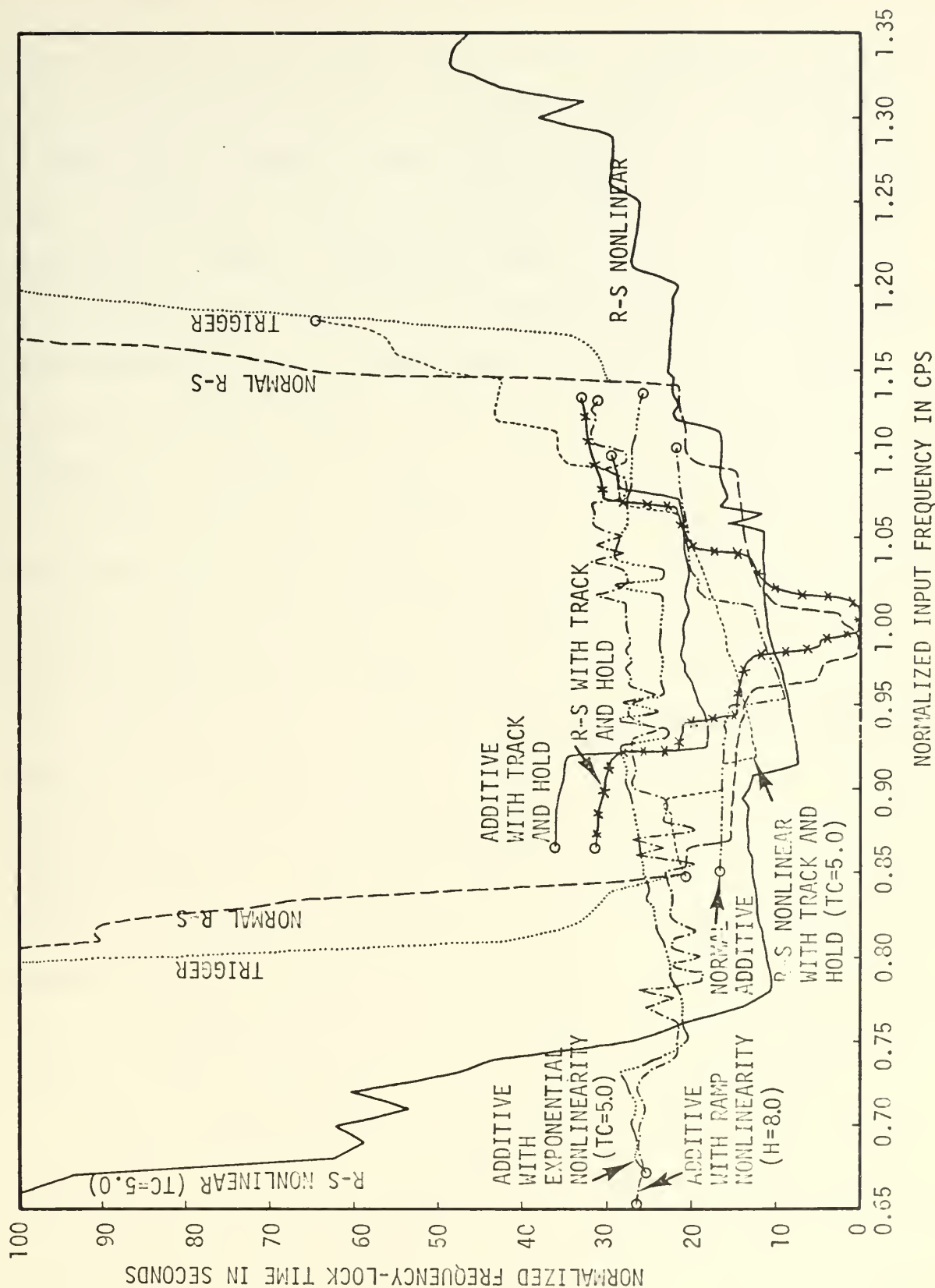


Figure V-I-1. Comparison of Frequency-Lock Time as a Function of Input Frequency for All Phase Comparators Using an Initial Phase of 180 Degrees.

factors which affect the shape of each curve it is necessary to consult the subsection which describes the operation of that phase comparator:

The range of frequencies over which each particular circuit will lock is also shown in Figure V-I-1, except that for three of the phase comparators no limiting frequency was found to exist within the range of frequencies investigated. An extended plot showing the lock performance characteristics over a wide range of input frequencies and lock times for the phase comparator circuits for which no limit was found in Figure V-I-1, is shown in Figure V-I-2 for the same operating conditions as in Figure V-I-1. It is seen from Figure V-I-2 that the R-S nonlinear phase comparator, which was first presented in this treatise, has a significantly reduced lock time for wide frequency deviations, which is a distinct advantage over all other types of phase comparators studied. This reduced lock time is a result of the nonlinear phase comparator's ability to provide an increase in gain when large phase errors exist, and yet maintain the same small signal gain and stability as the other phase comparators. Figure V-I-2 shows the exceptionally large range of frequencies over which lock could be attained using the R-S nonlinear phase comparator; and even in this figure, as in all other simulation results, there was no limiting frequency found for the lock range of the normal R-S, the trigger, and the R-S nonlinear phase comparators.

Another thorough overview of the system's operation with different types of phase comparators is provided in Figure V-I-3 which shows the normalized seize frequency, which is the frequency at which cycle skipping first occurs, for each type of phase comparator as a function of initial phase. This figure provides a clear picture of how each system can be expected to respond for various values of input phase, and since for several of the phase comparators studied the system will not lock once

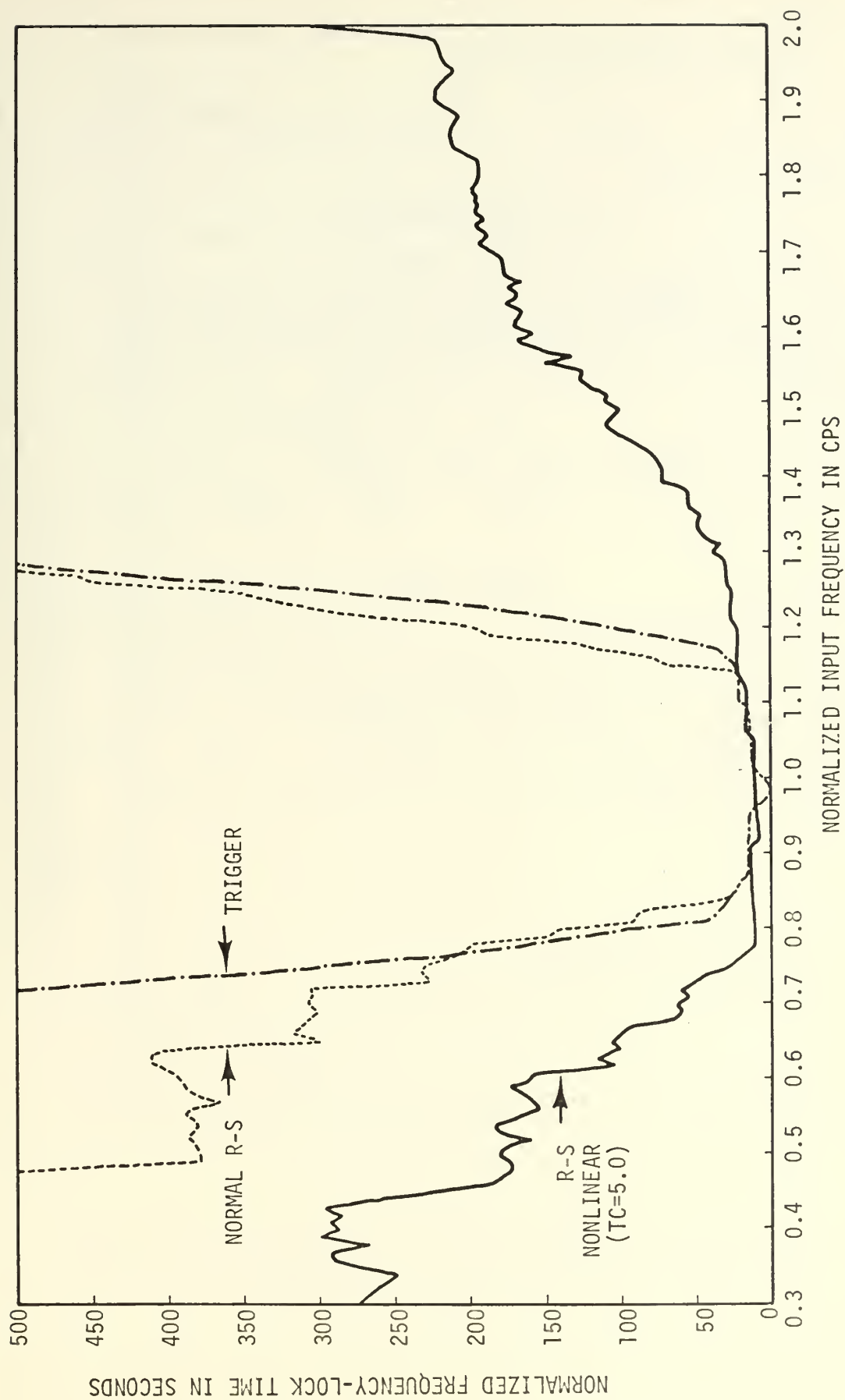


Figure V-I-2. Comparison of Frequency-Lock Times for Wide Variations of Input Frequency for Those Phase Comparators Which Always Attain Lock and Utilizing an Initial Phase of 180 Degrees.

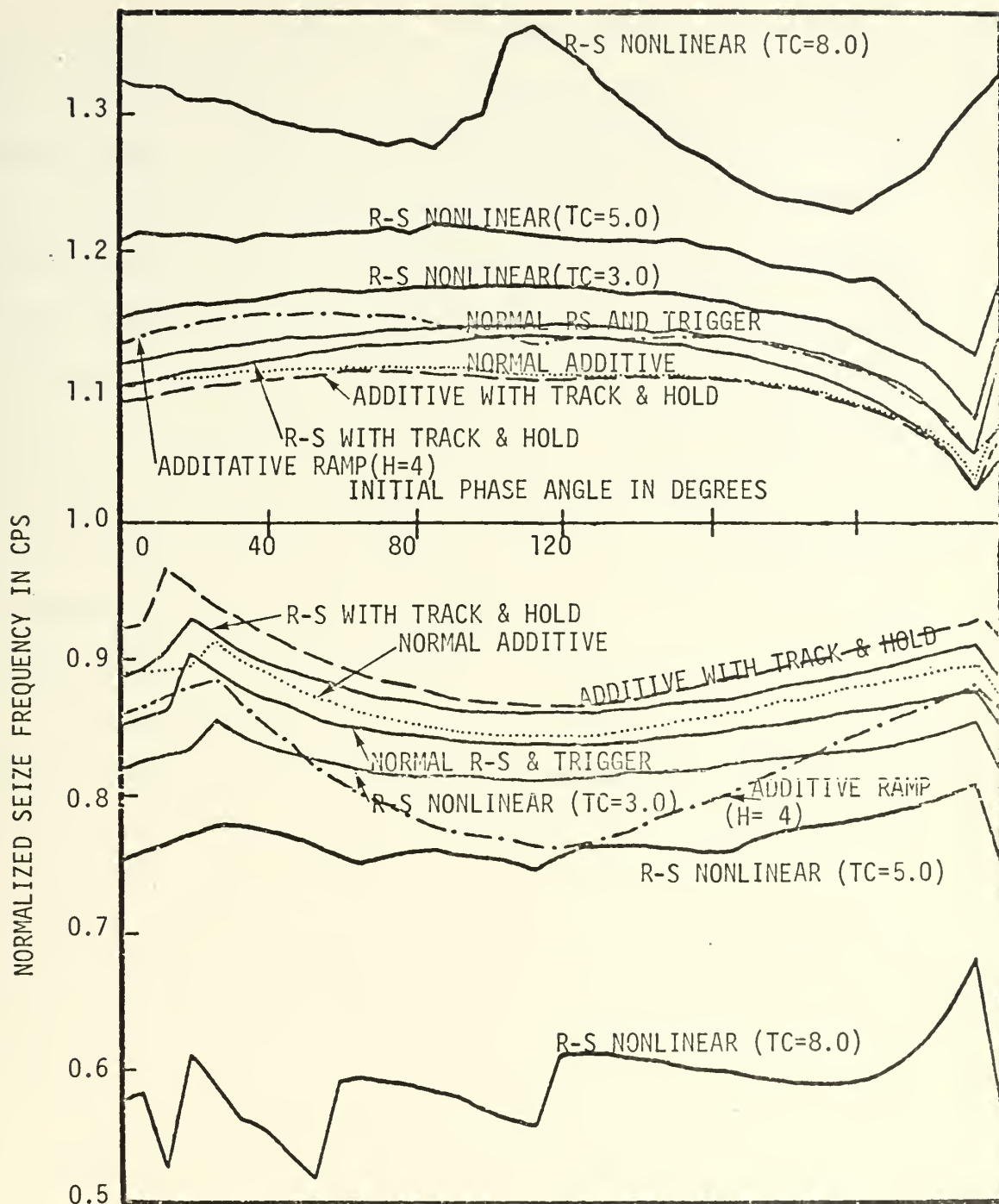


Figure V-I-3. Comparison of Normalized Seize Frequency as a Function of Phase for All Phase Comparators.

cycle skipping has occurred, then for these particular phase comparators the curves of Figure V-I-3 also indicate how the lock range varies with phase. Even for those phase comparator systems which will lock after cycle skipping has occurred, the data of Figure V-I-3 provides an approximate indication of lock times; since the time to lock always becomes greater each time an additional cycle is skipped. The curves of Figure V-I-3 also show some of the advantages of the R-S nonlinear circuit and portray the significantly wider range of frequencies over which this circuit will operate without cycle skipping. It can be noted in Figure V-I-3 that the curves for the normal R-S and the trigger phase comparator coincide, since the performance of these two circuits is identical up until the time of cycle skipping.

In addition to the curves already presented, Table V-I-1 has been prepared to list some of the principle characteristics that may be used as a basis of comparison when selecting the phase comparator for a particular application. It is realized that there is no single phase comparator which is best for all applications, but from the curves and data presented it can be seen that for circuit applications which require a short lock time over a wide range of frequency and phase variations, the R-S nonlinear phase comparator should be given serious consideration. An examination of the various curves provided in this subsection enable a cursory comparison to be made as to the advantages and disadvantages of each type of phase comparator, and then a more thorough examination can be made of any specific phase comparator desired using the data provided in the earlier portions of this section.

	R-S PHASE COMPARATOR	NONLINEAR R-S PHASE COMPARATOR	R-S PHASE COMPARATOR WITH TRACK AND HOLD	R-S NONLINEAR PHASE COMPARATOR WITH TRACK AND HOLD	TRIGGER PHASE COMPARATOR	ADDITIVE PHASE COMPARATOR	ADDITIVE PHASE COMPARATOR WITH TRACK AND HOLD	ADDITIVE NONLINEAR PHASE COMPARATOR
Is The System Free From Steady State Phase Errors?	YES	YES	YES	YES	YES	NO	NO	NO
Did the System Appear to Have an Unlimited Lock Range?	YES	YES	NO	NO	YES	NO	NO	NO
Could the System Continue Operation if the Input Signal Were Temporarily Interrupted?	NO	NO	YES	YES	YES	YES	YES	YES
Was the VCO Free of Instantaneous Frequency Variations in Steady State?	NO	NO	YES	YES	NO	YES	YES	YES
Could the System Attain Lock Even After Skipping a Cycle?	YES	YES	NO	SOME-TIMES	YES	SOME-TIMES	NO	SOME-TIMES
Was the System Relatively Free of Problems with Stability?	YES	YES	NO	NO	YES	YES	NO	YES

Table V-I-I. Principle Characteristics of the Various Types of Phase Comparators.

VI. CONCLUSIONS

The research of this thesis has investigated the operation of a third order type 2 phase-locked loop with a sawtooth phase comparator using both analog and digital simulation techniques employing an exact simulation of the system without making the usual continuous system approximations. All experimental work was carried out and the results presented in terms of normalized parameters so that the data might easily be applied to any operational situation.

The systems studied have included eight different forms of the sawtooth phase comparator of which two of the basic forms have been used previously and the rest are new with this work. Although all the phase comparators were designed to have the same small signal linear transfer function, the system performance was quite different depending upon the particular form of the phase comparator used, and as a result of the investigation the following conclusions have been reached:

1. Some of the phase-locked loops have only a limited range of frequencies over which the system will lock, while other systems have an unlimited lock range; and since the same linear transfer function was used for all systems, the basis for this difference in lock range lies in the nonlinear characteristics of the particular phase comparator used to determine the phase error of the system.

2. The deliberate insertion of the proper form of additional non-linearity into the phase comparator characteristics can significantly improve the system performance by yielding increased lock ranges, reduced lock times, and greater values of the seize frequency.

3. The ability of the system to attain lock after cycle skipping has occurred is dependent on the form of the phase comparator.

4. The initial phase relationship and frequency offset between the input and the VCO signals both affect the system's ability to lock and also the length of time required for the system to lock.

5. For some forms of the phase comparator the system operates with zero steady state phase error for all input frequencies, while for other forms of the phase comparator a steady state phase error exists whenever the input frequency is different from the VCO free running frequency.

6. For all systems the gain varies as a function of the input frequency; however, the type and amount of variation is quite different depending upon the form of the phase comparator used, and this variation in gain significantly affects the system's ability to lock and the time required to lock.

7. For some forms of phase comparators the system remains stable for all values of gain, while for other forms a point of system instability is reached as the gain is increased.

8. For any given form of phase comparator and set of initial conditions, the effect of variations in the system gain or filter parameters conforms closely with linear feedback theory, except for the phenomenon of cycle skipping.

9. The ability of the system to continue operating successfully if the input signal were temporarily interrupted is dependent upon the form of the phase comparator.

10. The presence and amount of instantaneous VCO frequency variation in steady state operation is dependent upon the form of the phase comparator used.

Many of the variations in system performance appear to be due to differences in the sample data effects produced by different forms of the phase comparator, and the system does not operate either as a true sample data system or as a true continuous system but rather as a mixture of the two forms. This sample data effect must be taken into consideration in any system design.

Areas in which additional work is required include the determination of the optimum form for the additional nonlinearity to be inserted into the system phase comparator in order to maximize the desired performance characteristics, and the determination of analytical expressions to adequately describe the system operation exactly without making restrictive approximations. Another area for further research is in determining the limits of stability of the systems, which might be accomplished with the use of Liapunov Functions.

CCCCCCCCCCCCCCCCCCCC

BASIC PHASE-LOCKED LOOP WITH R-S PHASE COMPARATOR

THE PRINCIPAL VARIABLES USED ARE LISTED BELOW:

DINFRE = FREQUENCY OF THE INPUT SIGNAL IN HERTZ
 DINPHA = PHASE OF INPUT SIGNAL IN DEGREES
 OUTFRQ = FREQUENCY OF THE VCO IN HERTZ
 AVGOUT = OUTPUT FREQUENCY AVERAGED OVER THE INPUT PERIOD
 GAIN = LOOP GAIN INCLUDING PHASE COMPARATOR, FILTER, AND VCO
 DT = ITERATION STEP SIZE IN SECONDS
 FINTIM = DURATION OF PROBLEM RUN TIME
 IPRINT = NUMBER OF ITERATION STEPS BETWEEN PRINTED OUTPUT
 CONV = CONVERGENCE CRITERION FOR FILTER INTEGRATION
 NCYCLE = NUMBER OF SKIPPED CYCLES
 TIMLOK = TIME AT WHICH THE SYSTEM ATTAINS FREQUENCY LOCK
 TPALOC = TIME AT WHICH THE SYSTEM ATTAINS PHASE LOCK
 Y = OUTPUT OF THE PHASE COMPARATOR

ALL COMPUTATIONS WILL BE PERFORMED IN DOUBLE PERCISION

```

IMPLICIT REAL*8(A-H,O-Z)
DIMENSION ARYOUT(420)
REAL*4 GTIME(900),GFREQ(900),GPHASE(900),LABEL1/4HFREQ/,
1 LABEL2/4HPHAS/,CNORM(900),CY(900),GINPUT(900),GVCO(900),
1 REAL*8 ITITLE(12),JOB WENAG333 LT,M,J,WENIGER
1 FREQUENCY AND PHASE ERROR VS TIME FOR A PLL

```

ESTABLISH THE INITIAL CONDITIONS

```

DINFRE=1.0
DINPHA=90.000
GAIN=0.00200
ZERC=0.02500
POLE=0.2500
DT=0.00500
FINTIM=45.000
IPRINT=100
PI=3.141592653589793
OUTFRQ=1.000
TIME=0.000
DZ=0.0
ANG=0.000
CCNV=1.00D-9
A=0.000
B=0.000

```

CC

WEN00010
 WEN00020
 WEN00030
 WEN00040
 WEN00050
 WEN00060
 WEN00070
 WEN00080
 WEN00090
 WEN00100
 WEN00110
 WEN00120
 WEN00130
 WEN00140
 WEN00150
 WEN00160
 WEN00170
 WEN00180
 WEN00190
 WEN00200
 WEN00210
 WEN00220
 WEN00230
 WEN00240
 WEN00250
 WEN00260
 WEN00270
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 WEN00890
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 WEN00910
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 WEN00930
 WEN00940
 WEN00950
 WEN00960

```

J=C
Y=-1.000
CINPOT=0.4
CVCO=1.0
ANORM=-1.0
Y1=C.000
Z=C.000
YIL=C.000
TIMLUK=C.000
TPALOC=C.000
PLOCK2=C.000
JG=C
GOUT=C.000
MB=C
MCYCLE=C
TLMCYC=C.000
PLOCK=C.000
AVGOUT=C.000
SAVGOU=C.000
K6=C
K7=C

      COMPUTE THE VALUES OF THE NONVARYING PARAMETERS

      PI2=2.000*PI
      DIFPH=(180.000 - DINPHA)/360.000
      PI=1.000/ZERO
      P2=1.000/POLE
      CINPD=1.000/DINFRE
      DINPRA=DINPHA*PI/180.000
      DINRAD=DINFRE*PI2
      ICOUNT=FINTIM/DT
      GDTIME=FINTIM/900.000
      PLOCK1=DINPD/2.000
      K4=DINPD/DT

      WRITE OUT THE VALUES OF THE SYSTEM VARIABLES

      WRITE(6,1003) GAIN
      WRITE(6,1004) DINFRE
      WRITE(6,1005) DINPHA

      BEGIN THE ITERATIVE SOLUTION OF THE PROBLEM

      DO 100 I=1, ICOUNT
      TIME=TIME + DT
  
```

C
 C
 C
 C
 C
 C
 C
 C


```

C      SIMULATE THE INPUT SIGNAL WAVEFORM
C      DINRA1=DINRAD*TIME + DINPRA
C      DINPUT=DSIN(DINRA1)
C
C      SIMULATE THE VCO SIGNAL WAVEFORM
C      OUTRAD=PI2*CUTFRQ
C      ANG=ANG + DT*OUTRAD
C      OUTPUT=DSIN(ANG)
C
C      SIMULATE THE PHASE COMPARATOR OPERATION
C      IF(A.GT.0.000) GO TO 31
C      IF(A*DINPUT.LT.0.000) GO TO 33
C      GO TO 31
C
C      ARRIVE AT THIS POINT WHEN EACH INPUT PULSE OCCURS
C
C      Y=1.0
C      ANORM=1.0
C      CINPUT=1.0
C      PLOCK1=TIME + DINPD/2.000
C      MA=1
C      IF(MA.NE.MB) GO TO 111
C      MCYCLE=MCYCLE + 1
C      TLMCYC=TIME
C      MB=MA
C      IF(B.GT.0.000) GO TO 32
C      IF(B*OUTPUT.LT.0.000) GO TO 34
C      GO TO 32
C
C      ARRIVE AT THIS POINT WHEN EACH VCO PULSE OCCURS
C
C      Y=-1.0
C      ANORM=-1.0
C      CVCO=1.0
C      MA=2
C      IF(MA.NE.MB) GO TO 110
C      MCYCLE=MCYCLE + 1
C      TLMCYC=TIME
C      MB=MA
C      PLOCK2=TIME
C      DIFPH=(PLOCK1 - PLOCK2)/DINPD
C      ABPLOC=DABS(DIFPH)
C      IF(ABPLOC.LT.0.0500*DINPD) GO TO 41
C      PLOCK=0.000
C      GO TO 43

```

```

WENCG970
WENCG980
WENCG990
WENCG1000
WENCG1010
WENCG1020
WENCG1030
WENCG1040
WENCG1050
WENCG1060
WENCG1070
WENCG1080
WENCG1090
WENCG1100
WENCG1110
WENCG1120
WENCG1130
WENCG1140
WENCG1150
WENCG1160
WENCG1170
WENCG1180
WENCG1190
WENCG1200
WENCG1210
WENCG1220
WENCG1230
WENCG1240
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WENCG1260
WENCG1270
WENCG1280
WENCG1290
WENCG1300
WENCG1310
WENCG1320
WENCG1330
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WENCG1370
WENCG1380
WENCG1390
WENCG1400
WENCG1410
WENCG1420
WENCG1430
WENCG1440

```



```

142      K5=I - K4 - K6
      SAVGOU=SAVGOU + OUTFRQ - ARYOUT(K5)
      AVGOUT=SAVGOU/K4
      ARYOUT(K5)=OUTFRQ
      K7=K7 + 1
      IF(K7.EQ.K4) GO TO 144
      GO TO 145
144      K6=K6 + K4
      K7=0
      CCNTINUE
145      CCNTINUE
143      C
      C
      C
      DETERMINE THE TIME AT WHICH FREQUENCY SYNCHRONIZATION OCCURS
      DELTF=OINFR - AVGOUT
      ADELTF=OABS(DELTF)
      IF(ADELTF.LT.O.O1DC) GO TO 13
      DLOCK=O.ODC
      GO TO 14
13      DLOCK=1.ODC
14      CCNTINUE
      C
      C
      C
      DETERMINE THE TIME AT WHICH PHASE SYNCHRONIZATION OCCURS
      IF(TPALOC.GT.O.ODC) GO TO 50
      IF(PLOCK.GT.O.9DC) GO TO 56
      TPALOC=O.ODC
      GO TO 57
56      TPALOC=TIME
      GO TO 57
50      IF(PLOCK.GT.O.9DC) GO TO 57
      TPALOC=O.ODC
      CCNTINUE
57      IF(TIMLOCK.GT.O.ODC) GO TO 30
      IF(DLOCK.GT.O.9DC) GO TO 16
      TIMLOCK=O.ODC
      GO TO 17
16      TIMLOCK=TIME
      GO TO 17
30      IF(DLOCK.GT.O.9DC) GO TO 17
      TIMLOCK=O.ODC
      CCNTINUE
17      C
      C
      C
      PERFORM PRINT OUT OPERATIONS AT THE PROPER INTERVAL
      J=J + 1
      IF(J.EQ.IPRINT) GO TO 60
      GO TO 61
WEN01930
WEN01940
WEN01950
WEN01960
WEN01970
WEN01980
WEN01990
WEN02000
WEN02010
WEN02020
WEN02030
WEN02040
WEN02050
WEN02060
WEN02070
WEN02080
WEN02090
WEN02100
WEN02110
WEN02120
WEN02130
WEN02140
WEN02150
WEN02160
WEN02170
WEN02180
WEN02190
WEN02200
WEN02210
WEN02220
WEN02230
WEN02240
WEN02250
WEN02260
WEN02270
WEN02280
WEN02290
WEN02300
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WEN02320
WEN02330
WEN02340
WEN02350
WEN02360
WEN02370
WEN02380
WEN02390
WEN02400

```



```

60 J=0
   WRITE(6,1001) TIME,DINPUT,OUTPUT,Y,Y1,OUTFRQ,AVGOUT,TIMLOK,
   1TPALOC
   WRITE(6,1006) MCYCLE,TLMCYC
   CONTINUE
61
C
C
C
C
   ARRANGE AND STORE THE INPUT AND VCO SIGNALS, THE PHASE COMPARATOR
   OUTPUT AND THE LOCK INDICATING FUNCTION FOR GRAPHIC OUTPUT
   IF(LOCK.GT.0.1) GO TO 6010
   DNORM=-0.4
   GO TO 6011
   DNORM=DLOCK - 0.95 - 0.4
6010 CCNTINUE
6011 IF(Y.GT.0.1) GO TO 6020
   DY=Y + 0.95 - 0.2
   GO TO 6021
   DY=Y - 0.95 - 0.2
6020 CCNTINUE
6021 IF(CINP.GT.0.9) CINP=CINP - 0.95 + 0.3
   IF(CVCO.GT.0.9) CVCO=CVCO - 0.95 + 0.2
   IF(TIME.GT.600) GO TO 74
   GO TO 75
   JG=JG + 1
   GOUT=GOUT + GDTIME
   GINPUT(JG)=CINPUT
   GVCO(JG)=CVCO
   CNORM(JG)=DNORM
   CY(JG)=DY
   CINP=0.3
   CVCO=0.2
   GPHASE(JG)=DINFRE - OUTFRQ
   GFREQ(JG)=DINFRE - AVGOUT
   GTIME(JG)= TIME
   CCNTINUE
75 CCNTINUE
100 WRITE(6,2001)
C
C
C
C
   PLOT OUT THE SPECIFIED SYSTEM PARAMETERS
   CALL PLOTP(GTIME,GFREQ,900,0)
   WRITE(6,2001)
   CALL PLOTP(GTIME,GPHASE,900,0)
   CALL DRAW(900,GTIME,GFREQ,1,0,LABEL1,ITITLE,5.0,2,5,0,2,2,9,10,
   10,LAST1)
   CALL DRAW(900,GTIME,GINPUT,2,0,LABEL2,ITITLE,5.0,2,5,0,
   12,2,0,10,C,LAST2)
   CALL DRAW(900,GTIME,GVCO,2,0,LABEL2,ITITLE,5.0,2,5,0,

```



```

12,2,9,10,0, LAST2)
CALL DRAW(900,GTIME,CNORM,2,0,LABEL2,ITITLE,5,2,5,0,
12,2,9,10,0, LAST2)
CALL DRAW(900,GTIME,CY,2,0,LABEL2,ITITLE,5,2,5,0,
12,2,9,10,0, LAST2)
CALL DRAW(900,GTIME,GPHASE,3,0,LABEL2,ITITLE,5,2,5,0,
12,2,9,10,0, LAST2)
FCRMAP(I2F11,5)
1001 FORMAT(//,10F10.5,/)
1002 FORMAT(//,GAIN=,F10.5)
1003 FORMAT(//,INPUT FREQUENCY =,F10.5)
1004 FORMAT(//,INPUT PHASE=,F10.5)
1005 FORMAT(//,F11.5)
1006 FORMAT(I24,F11.5)
2001 STOP
773 END

```


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KEY WORDS	LINK A		LINK B		LINK C	
	ROLE	WT	ROLE	WT	ROLE	WT
Phase-Locked Loop Phase Controlled Oscillator Phase Synchronization Phase Comparators						

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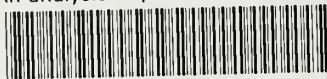
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